

COMPAL CONFIDENTIALMODEL NAME : **JAL21**PCB NO : **LA-4042P (DAA00000T0L)**BOM P/N : **43153331L01****M09 Maybach DIS
uFCPGA Mobile Penryn
Intel Cantiga PM + ICH9M****2007-10-30****REV : 0.1****@ : Nopop Component**

MB PCB

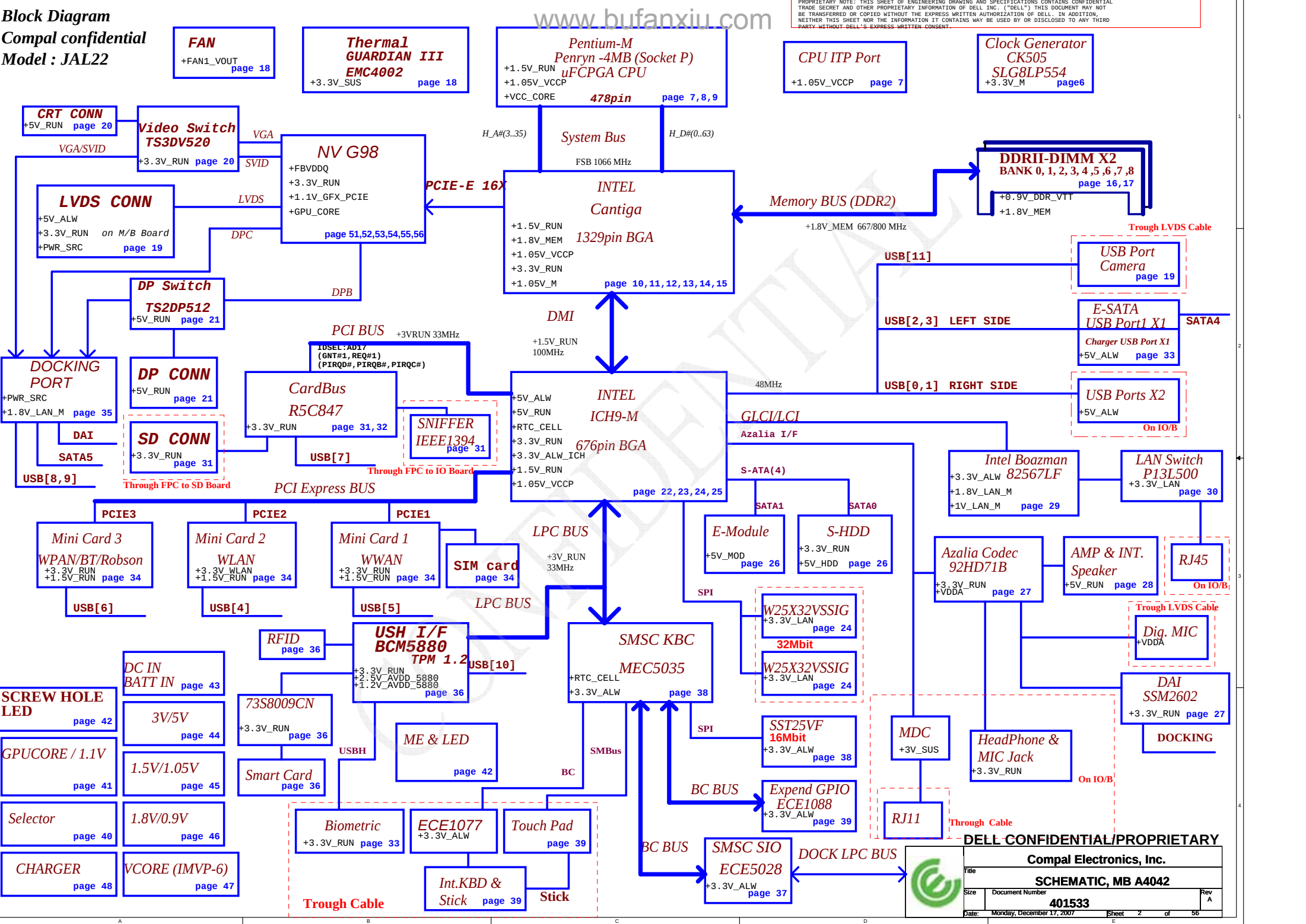
Part Number	Description
DAA00000R0L	PCB 83P LA-4051P REV0 M/8

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Block Diagram
Compal confidential
Model : JAL22



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State power plane	+15V_ALW +5V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO	+3.3V_SUS +1.8V_MEM	+5V_RUN +3.3V_RUN +2.5V_RUN +1.5V_RUN +0.9V_DDR_VTT +GPU_CORE +VCC_CORE +1.05V_VCCP +FBVDDQ +1.1V_GFX_PCIE	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C847	AD17	REQ#1 / GNT#1	PIRQ[B..D]

ICH9-M	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Bottom)
	3	JESA1 (Ext Left Side TOP)
	4	WLAN
	5	WWAN
	6	WPAN
	7	Card Bus/Express card
	8	DOCKING
	9	DOCKING
	10	USH->BIO
	11	Camera

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 BT/UWB
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	10/100/1G LAN

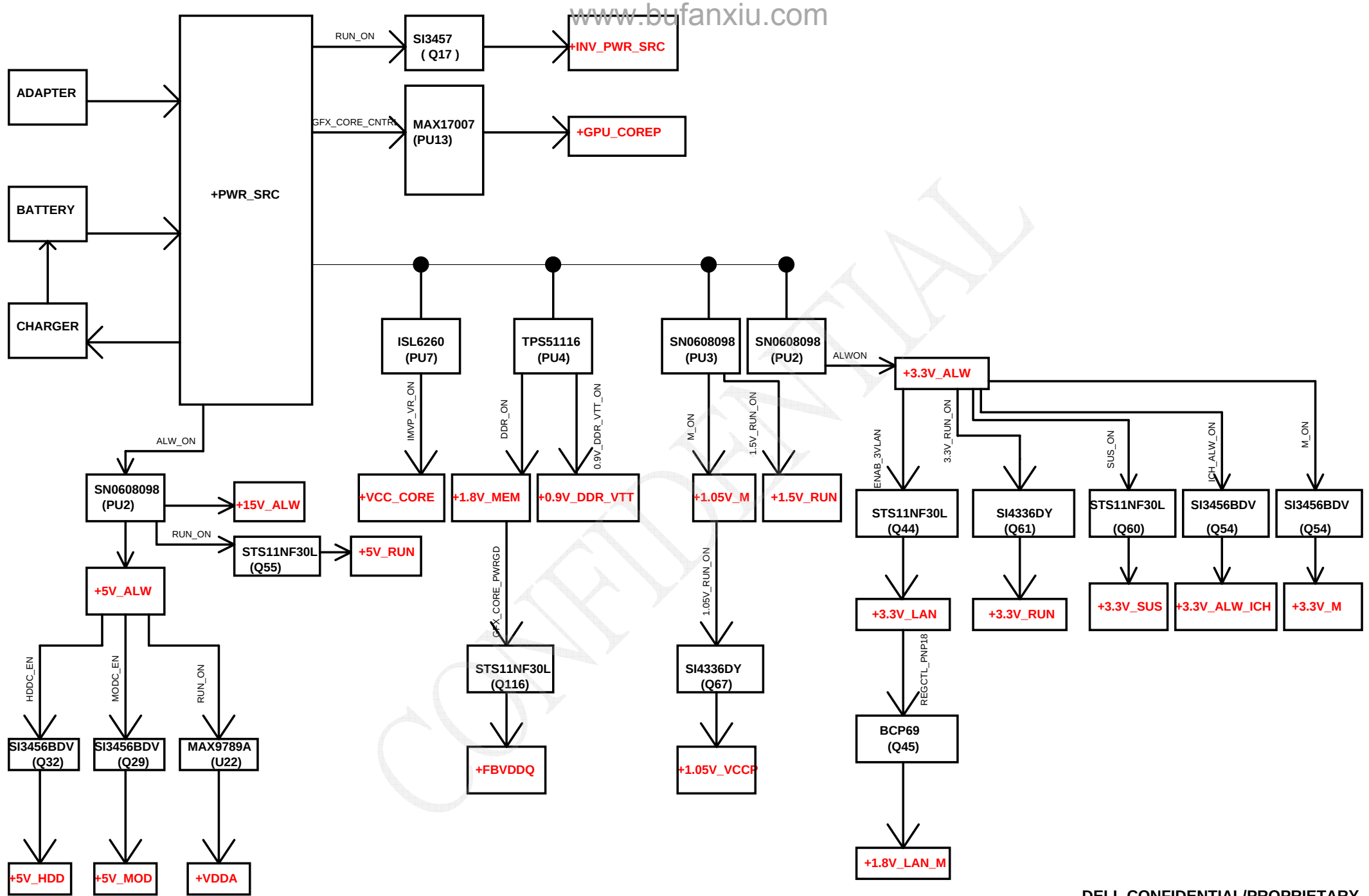
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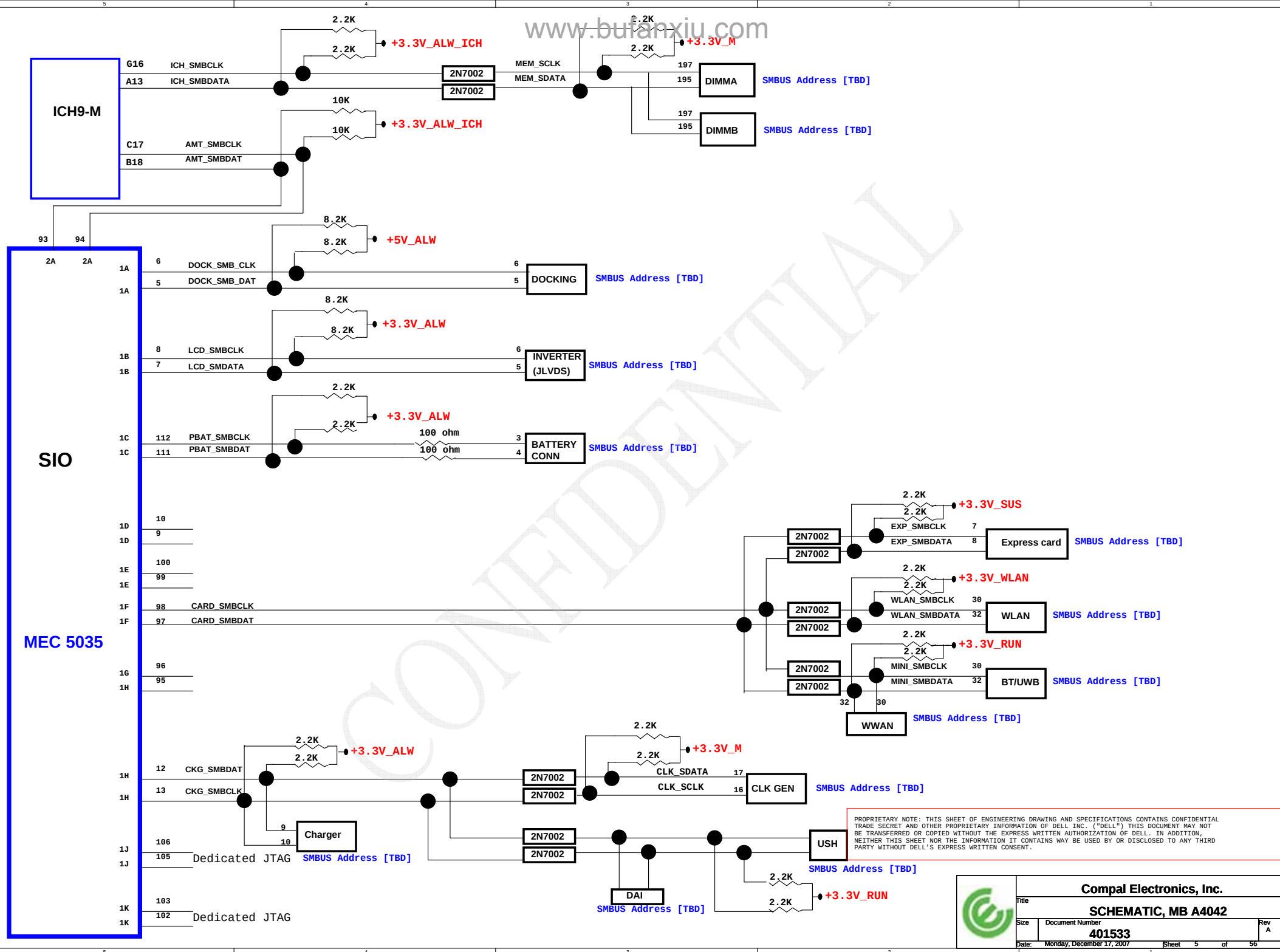
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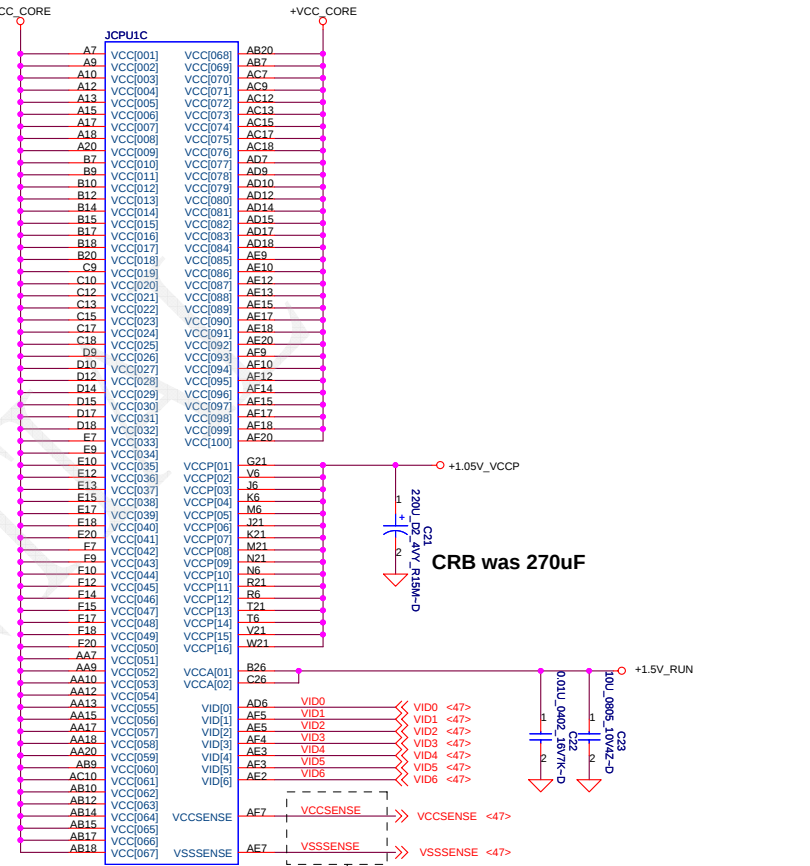
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Length match within 25 mils, Z0=27.4 ohm

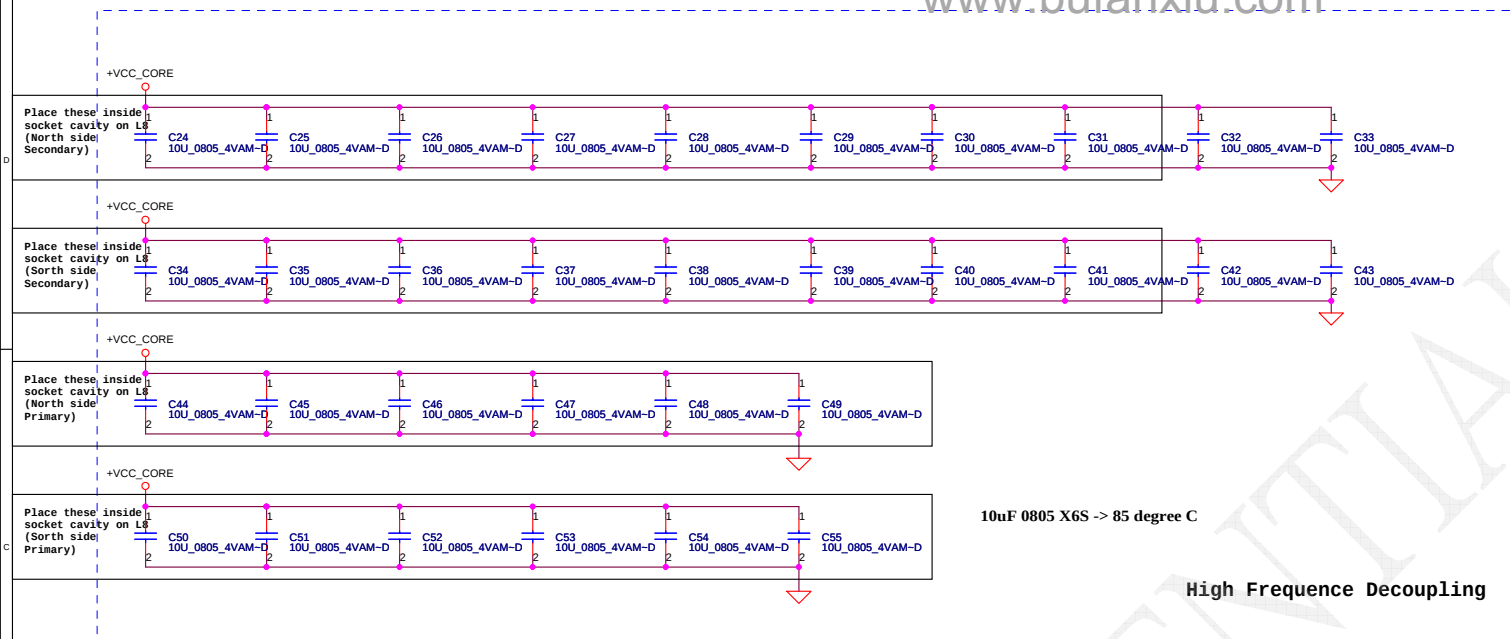
Place R75 and R76 near CPU

Route VCCSENSE and VSSSENSE trace at
27.4 ohms, 7 mils spacing and the placement should be within 1 inch (max)

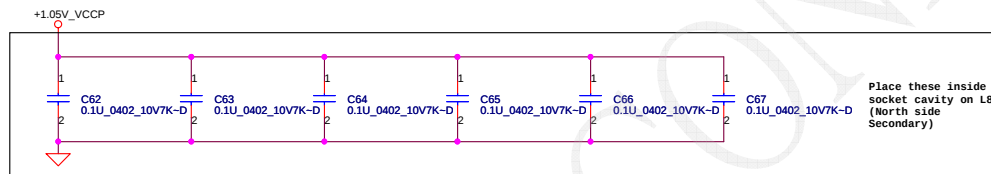
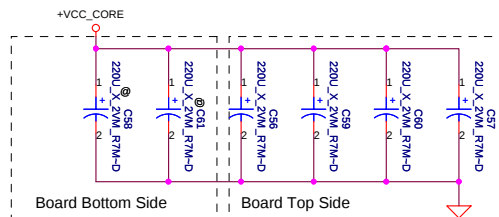
Layout close CPU PIN AD
50 ohm, 0.5 inch (max)



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Near VCORE regulator.

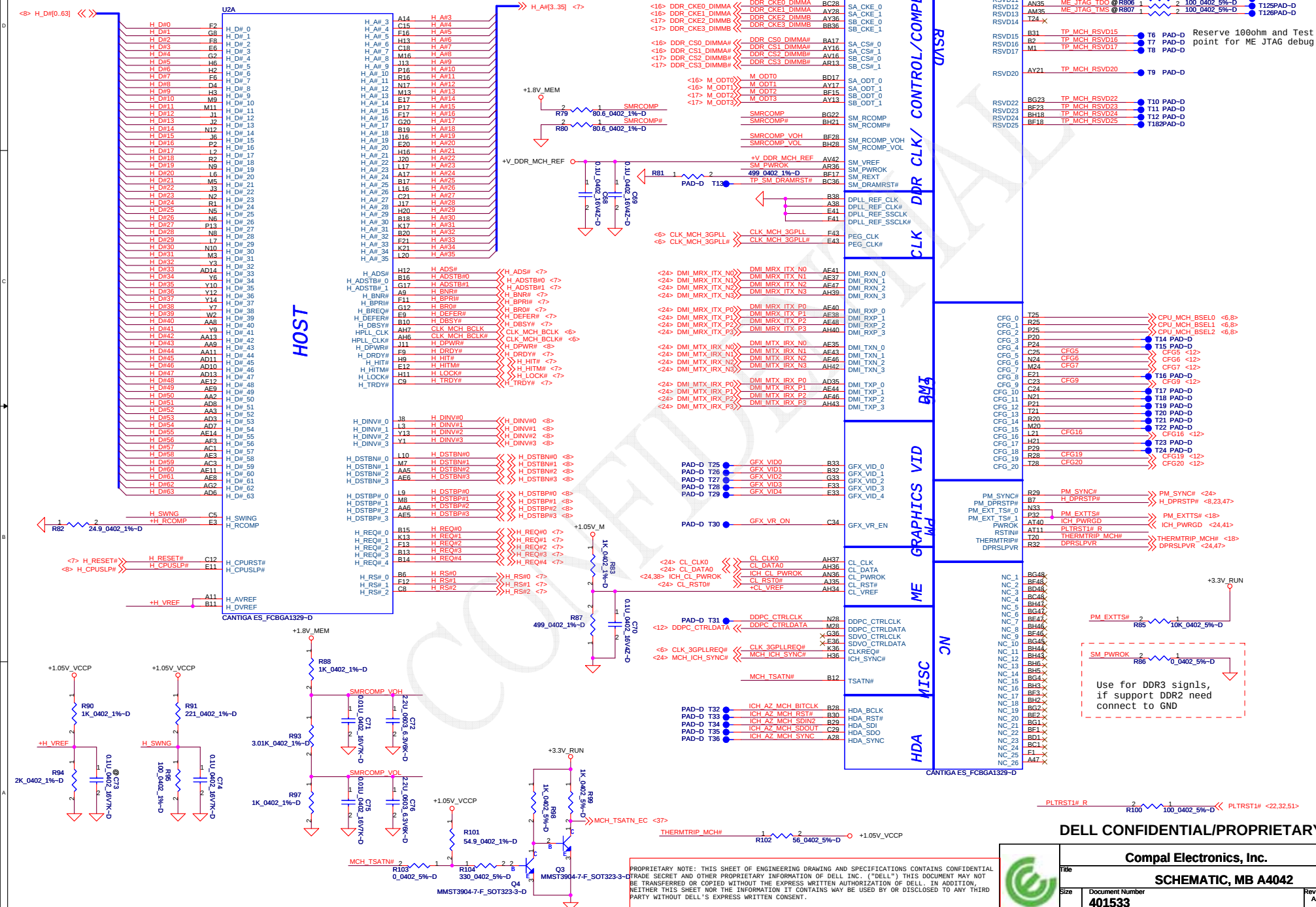


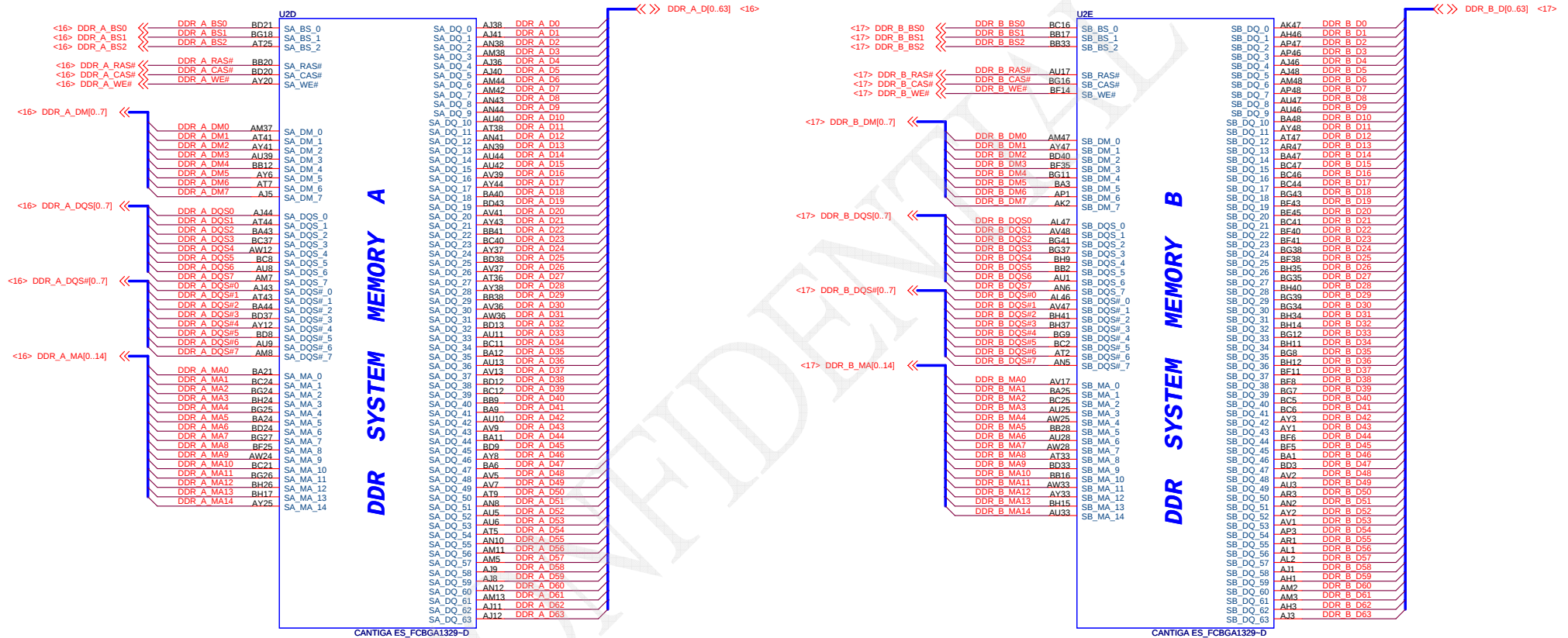
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CANTIGA ES_FCBGA1329-D

CANTIGA ES_FCBGA1329-D

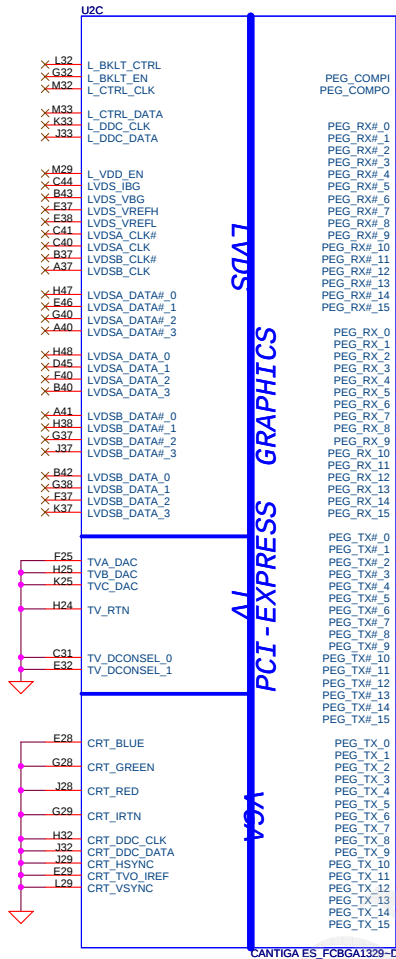
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PEG_COMP1
PEG_COMP0PEG_RX#_0
PEG_RX#_1
PEG_RX#_2
PEG_RX#_3
PEG_RX#_4
PEG_RX#_5
PEG_RX#_6
PEG_RX#_7
PEG_RX#_8
PEG_RX#_9
PEG_RX#_10
PEG_RX#_11
PEG_RX#_12
PEG_RX#_13
PEG_RX#_14
PEG_RX#_15PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15PEG_TX#_0
PEG_TX#_1
PEG_TX#_2
PEG_TX#_3
PEG_TX#_4
PEG_TX#_5
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PEG_TX#_7
PEG_TX#_8
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PEG_TX#_10
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PEG_TX#_12
PEG_TX#_13
PEG_TX#_14
PEG_TX#_15PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15

CANTIGA ES_FCBGA1328-D

+VCC_PEG
R105
49.9_0402_1%-D

T37

T36

PEGCOMP

PEGCOMP

H44

J46

L44

L40

N41

P48

N44

T43

Y43

Y48

Y36

AA43

AD37

AC47

AD39

H43

J44

L43

L41

N40

P47

N43

T42

Y42

Y42

W47

Y37

AA42

AD36

AC48

AD40

J41

M46

M47

M40

M42

R48

N38

T40

U37

U40

Y40

AA46

AA37

AD43

AC46

J42

L46

M48

M39

M43

R47

N37

T39

U36

U39

Y39

Y46

AA36

AA39

AD42

AD46

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PEG_MTX_GRX_C_N0 C78 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_N0

PEG_MTX_GRX_C_P1 C79 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_P1

PEG_MTX_GRX_C_N1 C80 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_N1

PEG_MTX_GRX_C_P2 C81 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_P2

PEG_MTX_GRX_C_N2 C82 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_N2

PEG_MTX_GRX_C_P3 C83 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_P3

PEG_MTX_GRX_C_N3 C84 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_N3

PEG_MTX_GRX_C_P4 C85 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_P4

PEG_MTX_GRX_C_N4 C86 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_N4

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PEG_MTX_GRX_C_N6 C90 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_N6

PEG_MTX_GRX_C_P7 C91 2 1 0.1U 0402 10V7K-D PEG_MTX_GRX_P7

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PEG_MTX_GRX_C_P14 C105 1 2 0.1U 0402 10V7K-D PEG_MTX_GRX_P14

PEG_MTX_GRX_C_N14 C106 1 2 0.1U 0402 10V7K-D PEG_MTX_GRX_N14

PEG_MTX_GRX_C_P15 C107 1 2 0.1U 0402 10V7K-D PEG_MTX_GRX_P15

PEG_MTX_GRX_C_N15 C108 1 2 0.1U 0402 10V7K-D PEG_MTX_GRX_N15

Strap Pin Table

CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG6	iTPM Host Interface	Low = iTPM enable High = iTPM disable(Default)
CFG7	Management Engine Crypto Strap	Low = TLS cipher suite with no confidentiality High = TLS cipher suite with confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	Digital Display Port Concurrent Operation	Low=Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port
SDVO_CTRL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present
DDPC_CTRLDATA		Low=DisplayPort disabled (default) High=DisplayPort device present

<10> CFG5 >> @R106 1 2 2.21K 0402 1%-D

<10> CFG6 >> @R107 1 2 2.21K 0402 1%-D

<10> CFG7 >> @R108 1 2 2.21K 0402 1%-D

<10> CFG9 >> @R109 1 2 2.21K 0402 1%-D

<10> CFG16 >> @R110 1 2 2.21K 0402 1%-D

CFG[5:16] have internal pullup

<10> CFG19 >> @R111 1 2 4.02K 0402 1%-D

<10> CFG20 >> @R112 1 2 4.02K 0402 1%-D

<10> DDPC_CTRLDATA >> @R113 1 2 4.02K 0402 1%-D

CFG[19:20] have internal pulldown

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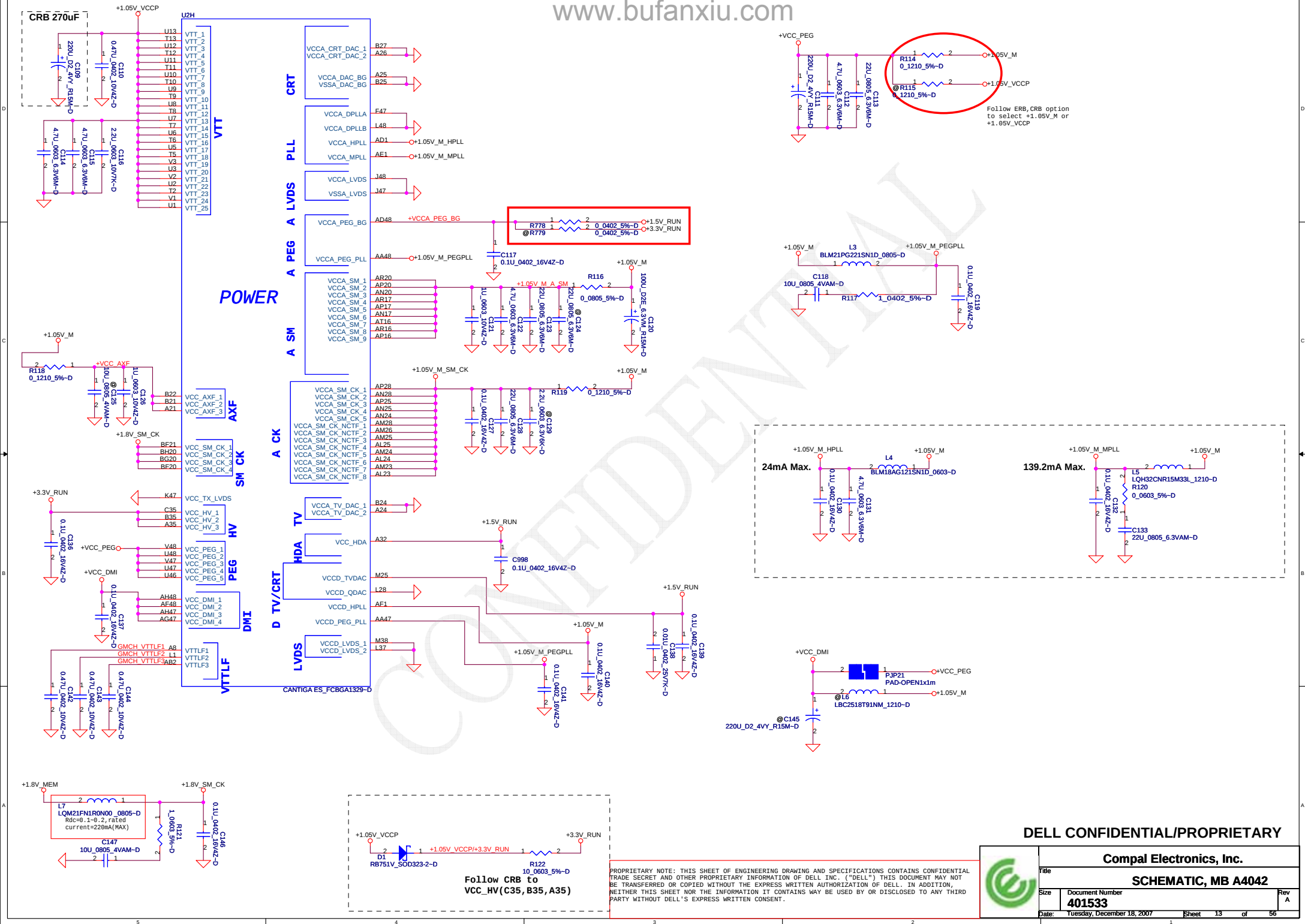
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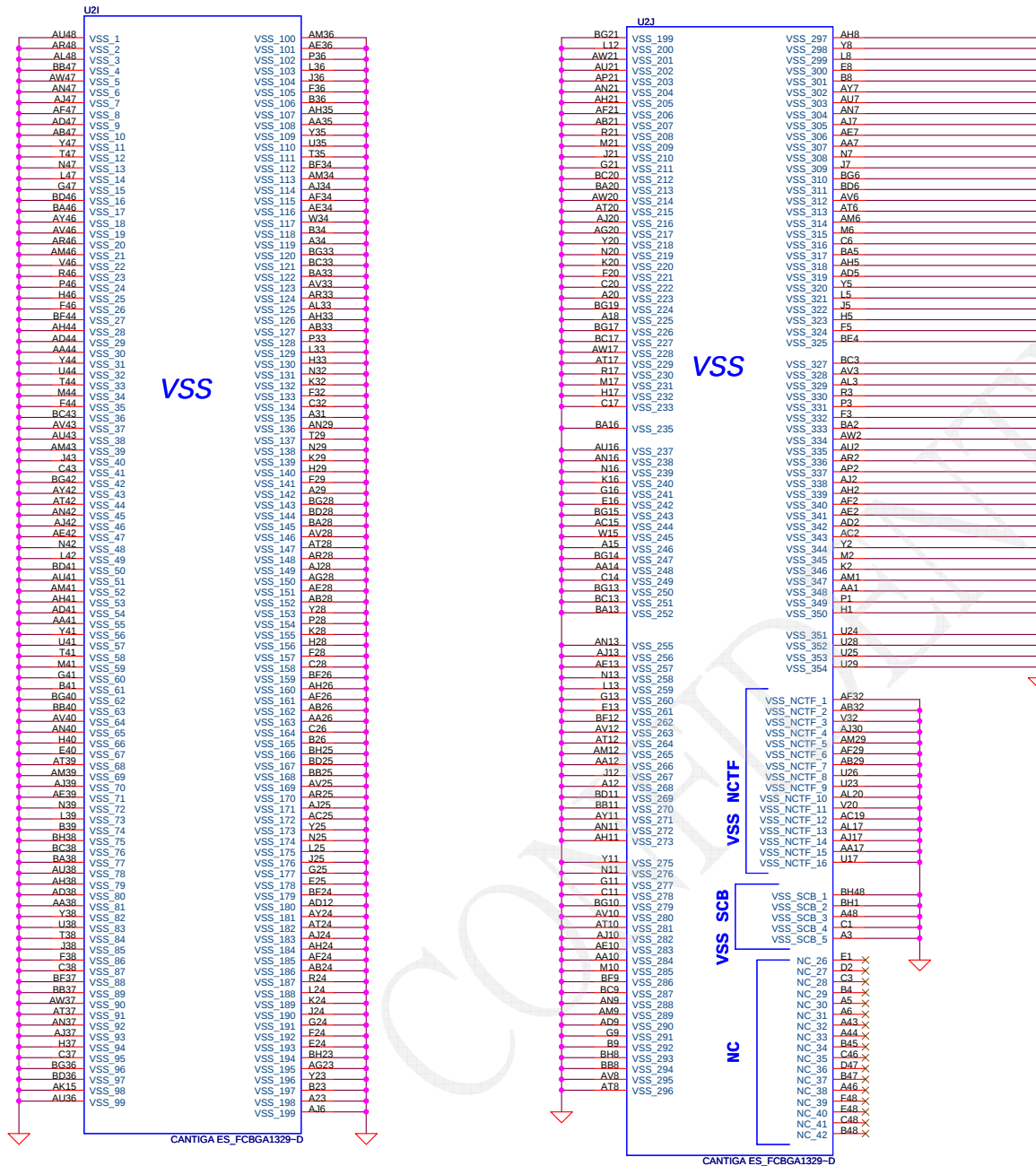
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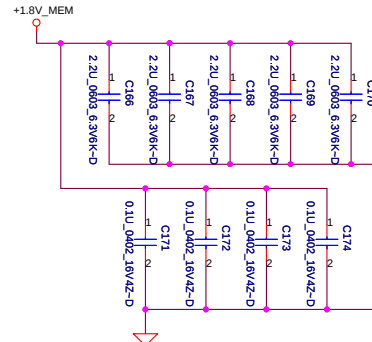
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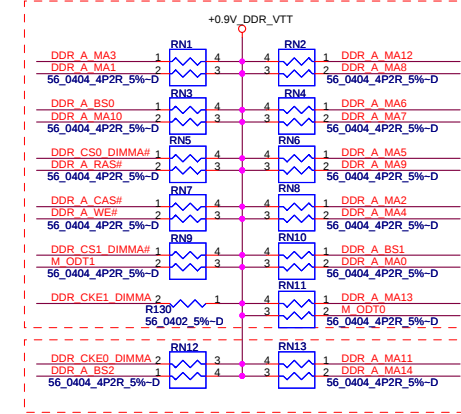
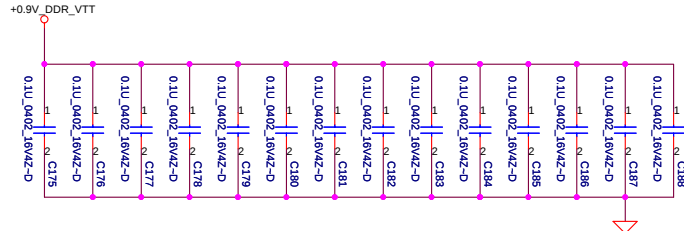
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<11> DDR_A_DQS#[0..7] <<>>
 <11> DDR_A_D[0..63] <<>>
 <11> DDR_A_DM[0..7] <<>>
 <11> DDR_A_DQS#[0..7] <<>>
 <11> DDR_A_MA[0..14] <<>>

Layout Note:
Place near JDIMMA

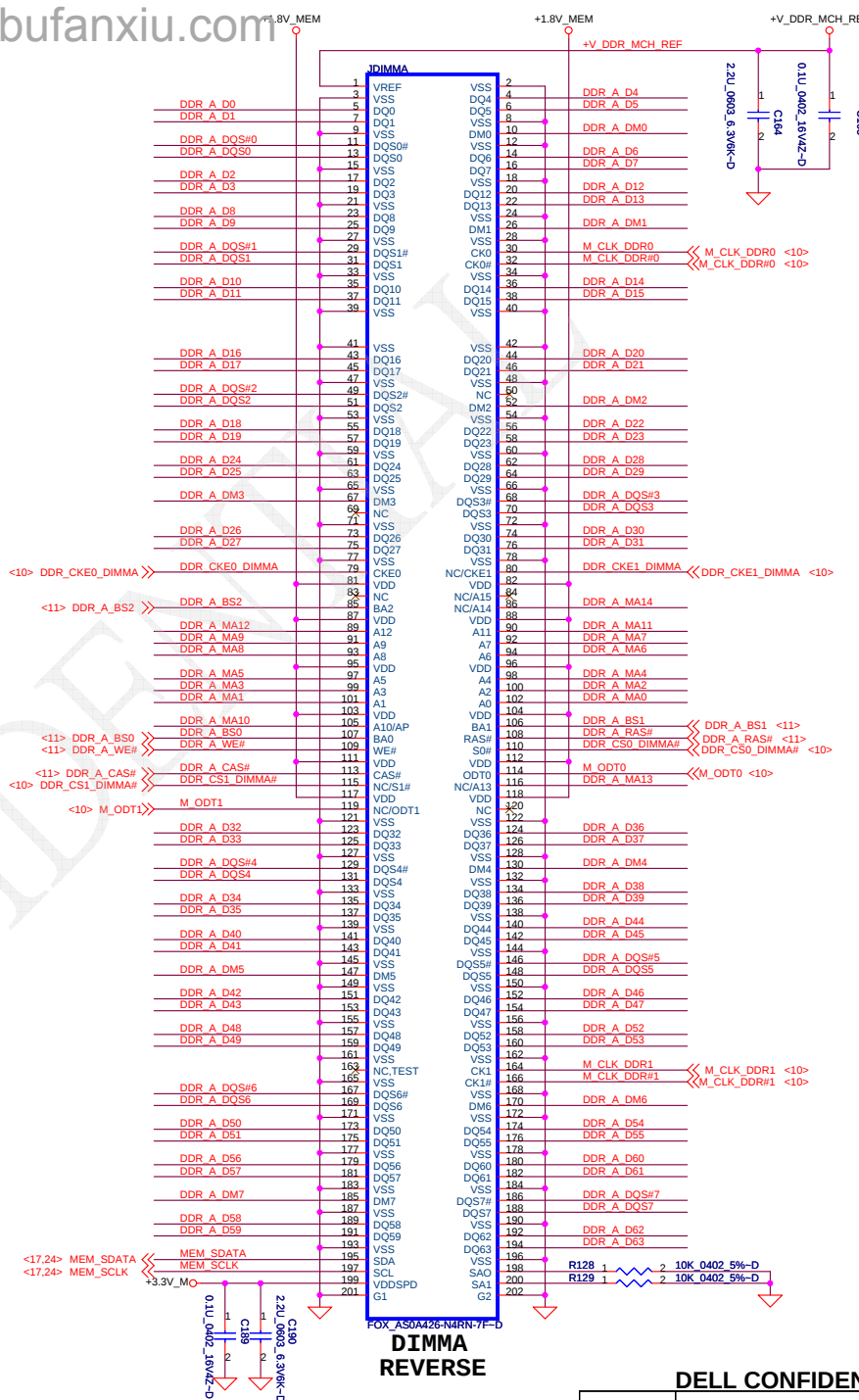


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor
closely JDIMMA, all
trace length<750 mil

Layout Note:
Place these resistor
closely JDIMMA, all
trace length
Max=1.3"



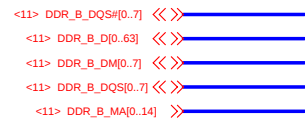
DIMMA
REVERSE

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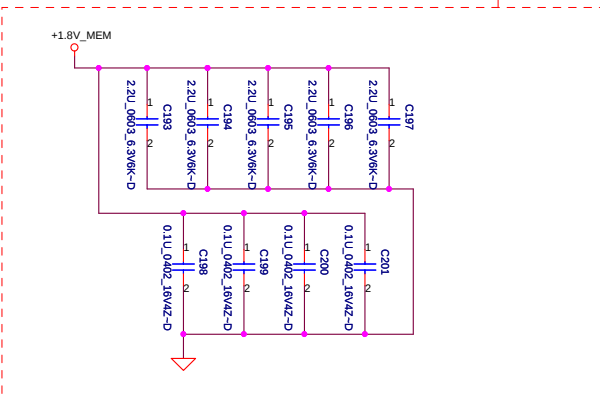


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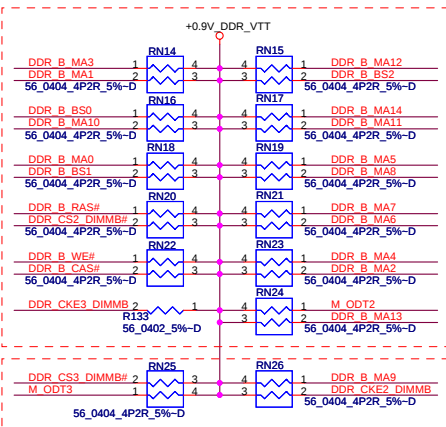
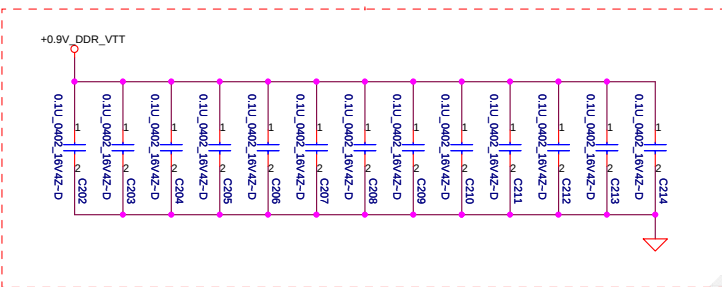
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Layout Note:
Place near JDIMMB

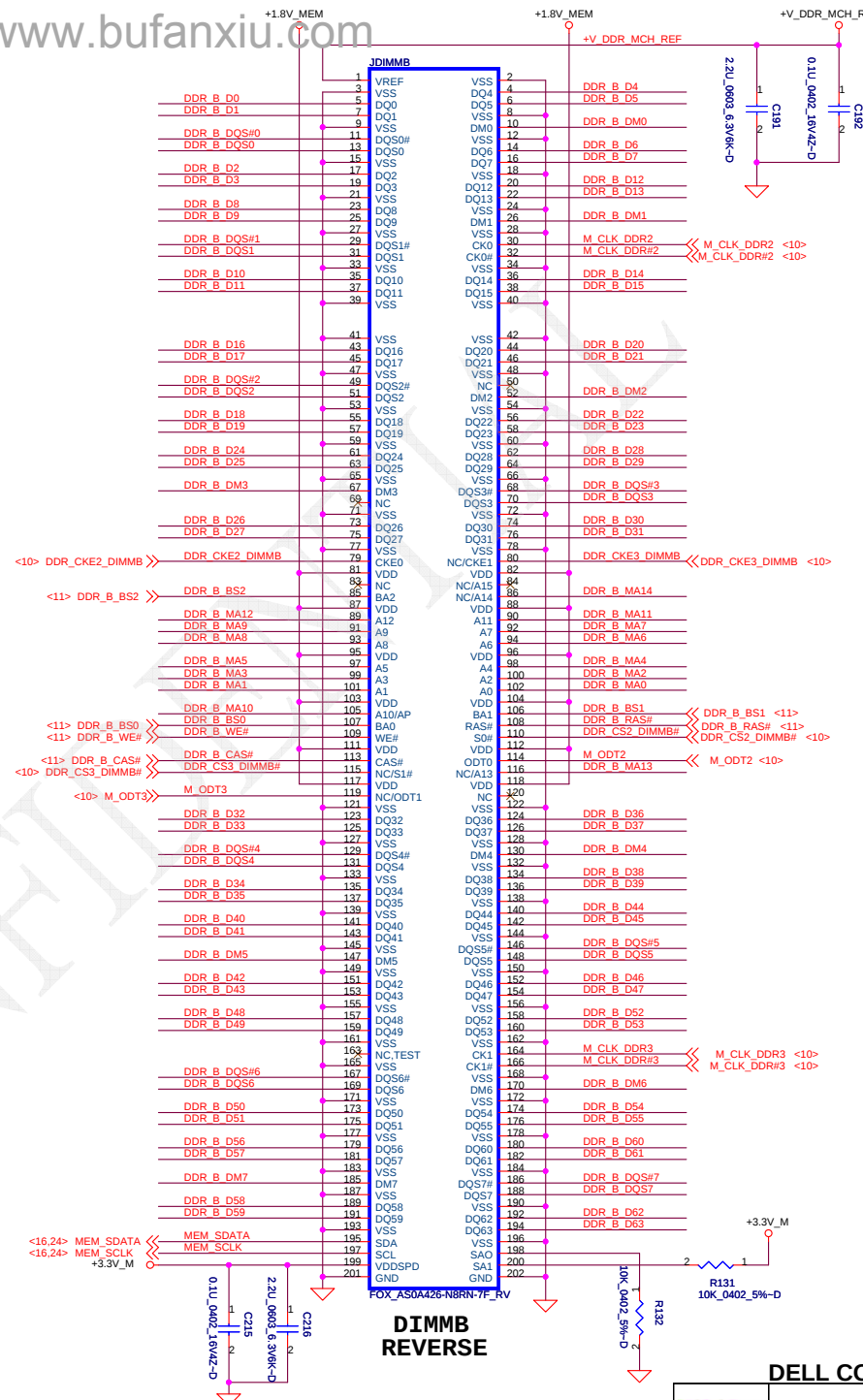


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Layout Note:
Place these resistor
closely JDIMMB,all
trace length<750 mil

Layout Note:
Place these resistor
closely JDIMMB, all
trace length
Max=1.3"



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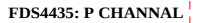
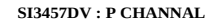
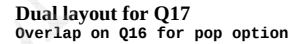
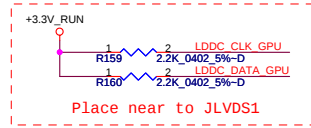
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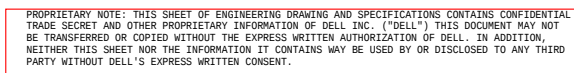
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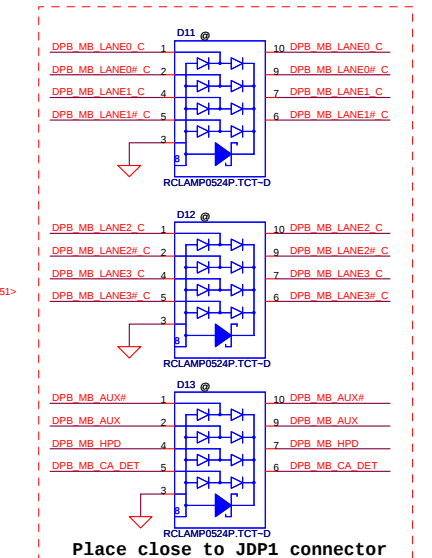
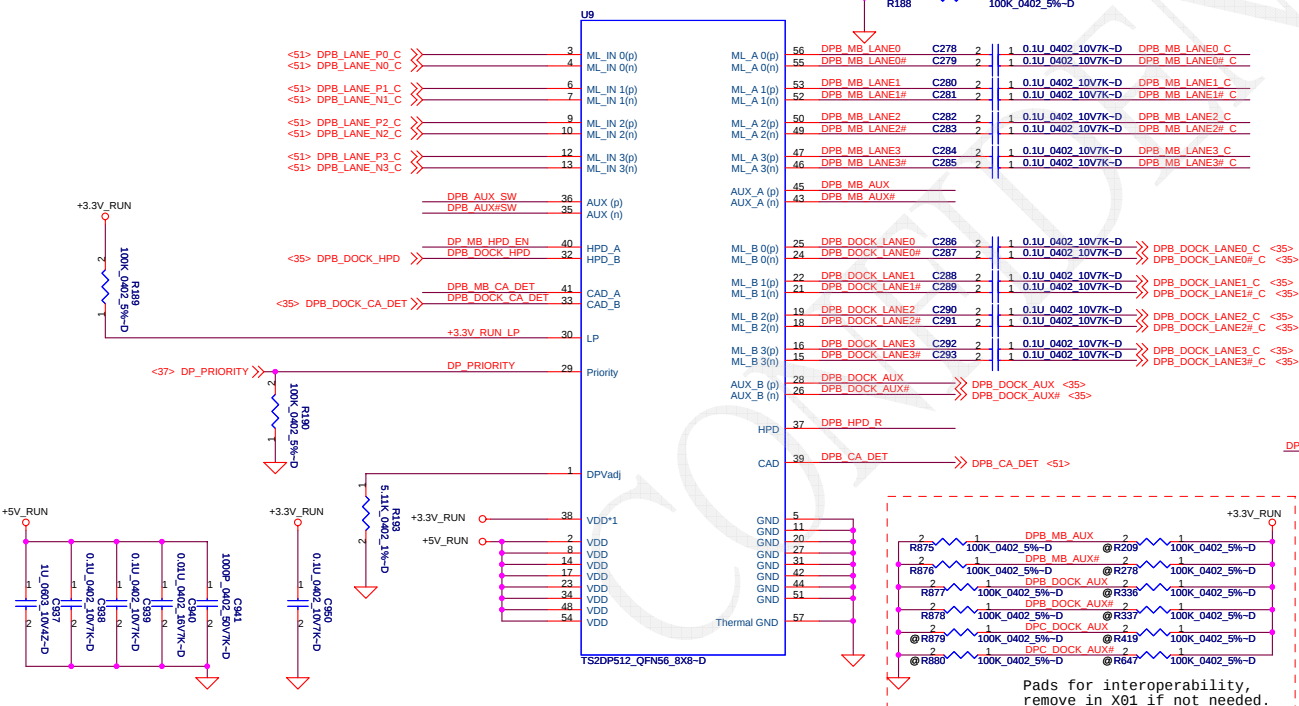
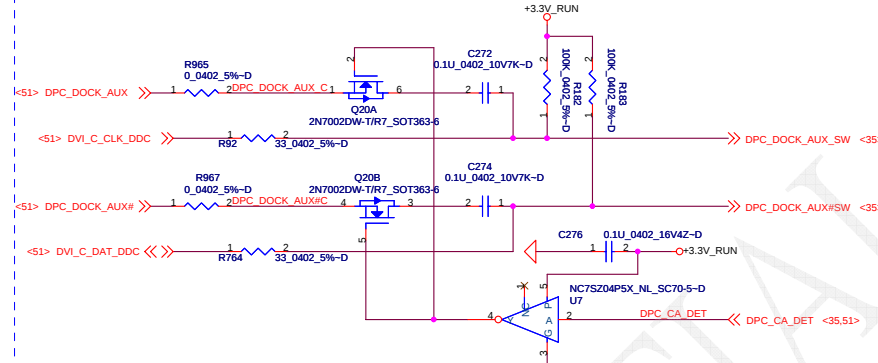
Date: Tuesday, December 18, 2007 Sheet 18 of 56



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SW for eDOCK side



Pin30	Level	State	Description
LP	Hi	Normal Mode	Standard operational mode for device
	Low	Low power Mode	Device is forced into a low power mode causing the output s to go to a high-Z state, all other inputs are ignore

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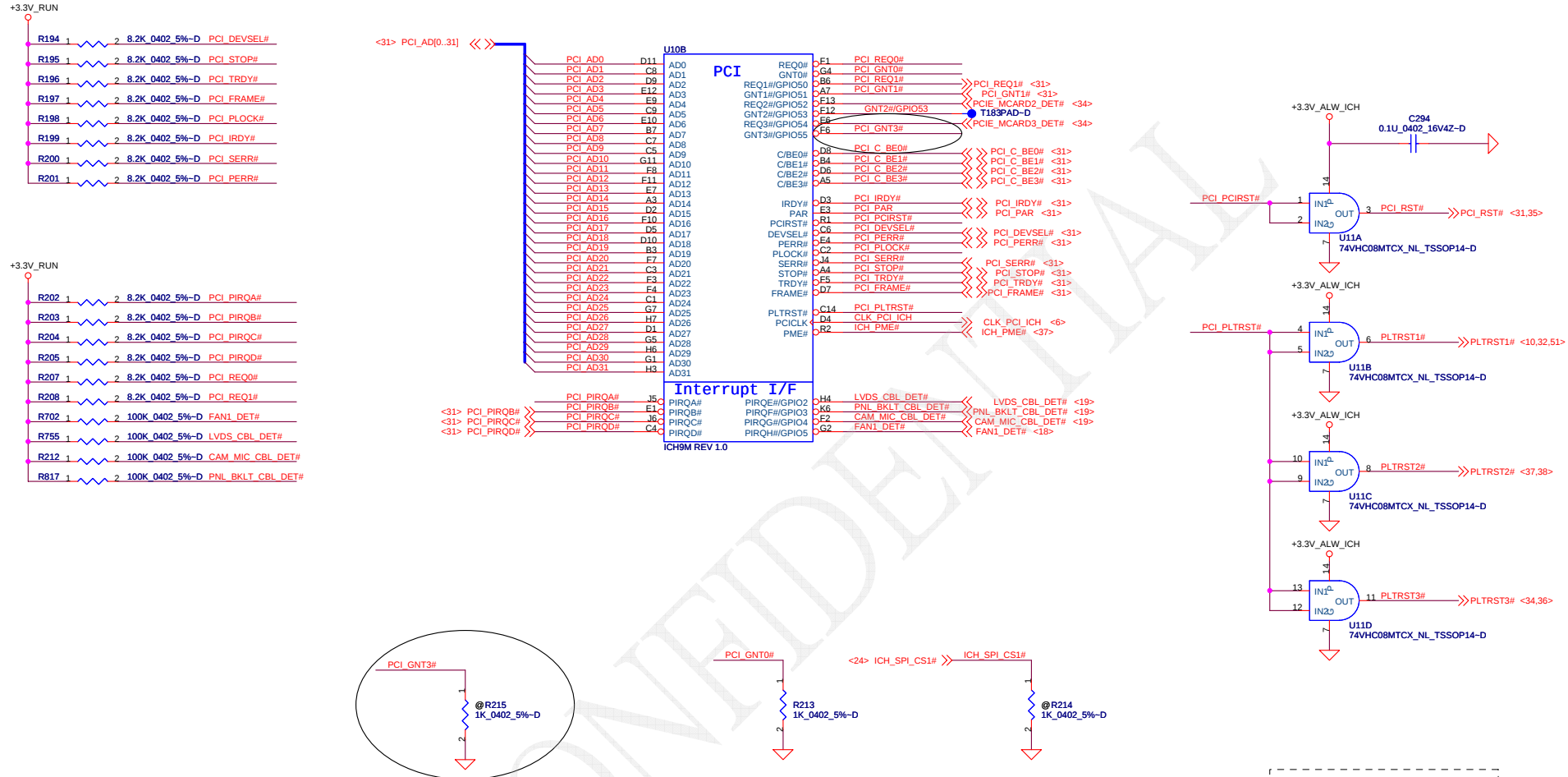
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SCHEMATIC, MB A4042

101502

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A16 away override strap.

PCI_GNT3#/(MDC_RST_DIS#)	Low = A16 swap override enabled. High = Default. pull up internal
--------------------------	--

Boot BIOS Strap

PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC

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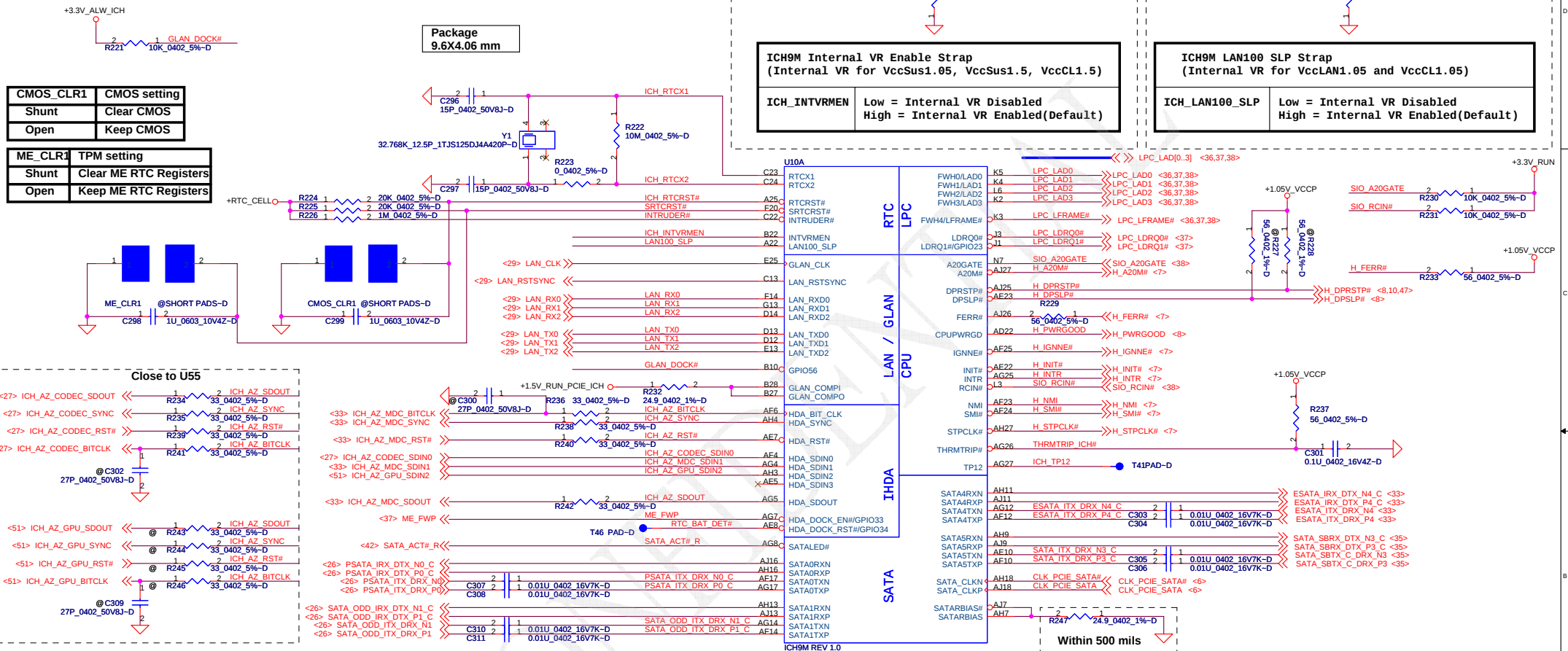
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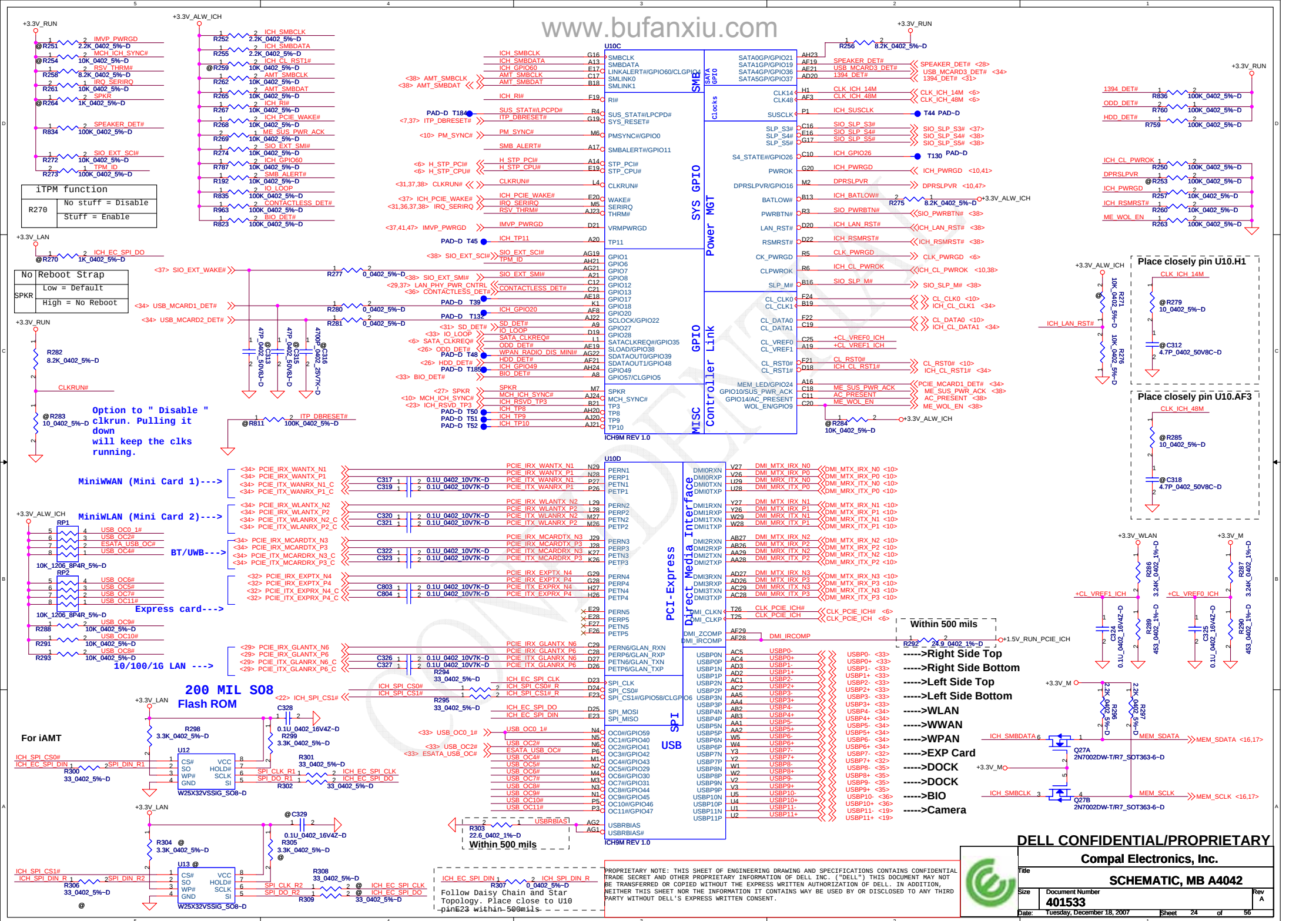
Date	Tuesday, December 18, 2007	Sheet	22	of	56
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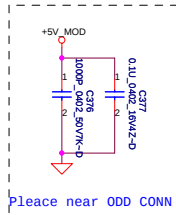


XOR Chain Entrance Strap			
ICH	RSVD_TP3	HDA SDOOUT	Description
	0	0	RSVD
	0	1	Enter XOR Chain
	1	0	Normal Operation (Default)
	1	1	Set PCIE port config bit 1

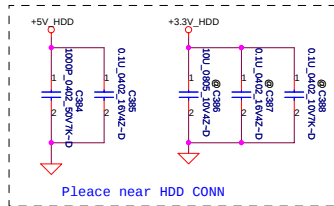
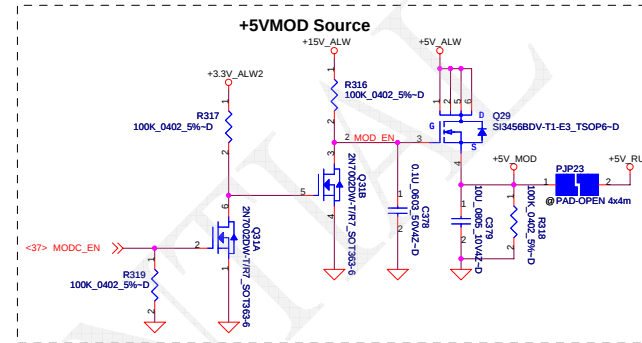
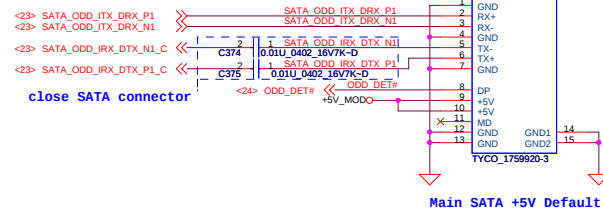
R375, R961, R960, R962 Q130 remove for RTC detect function



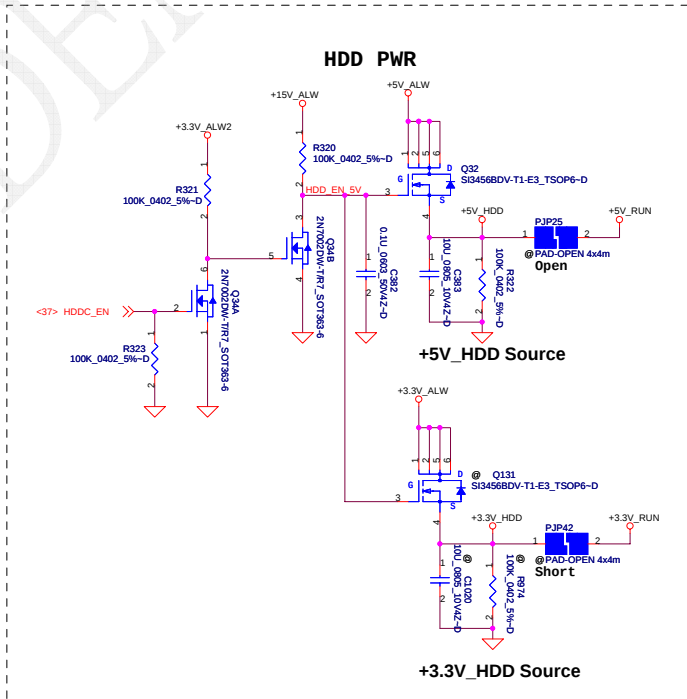
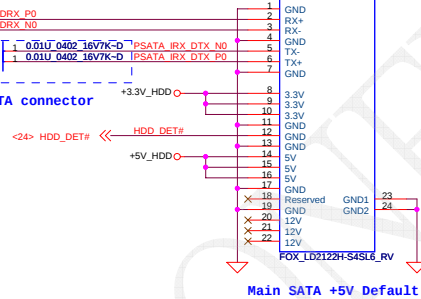




For ODD



For HDD

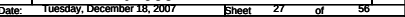


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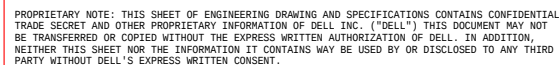
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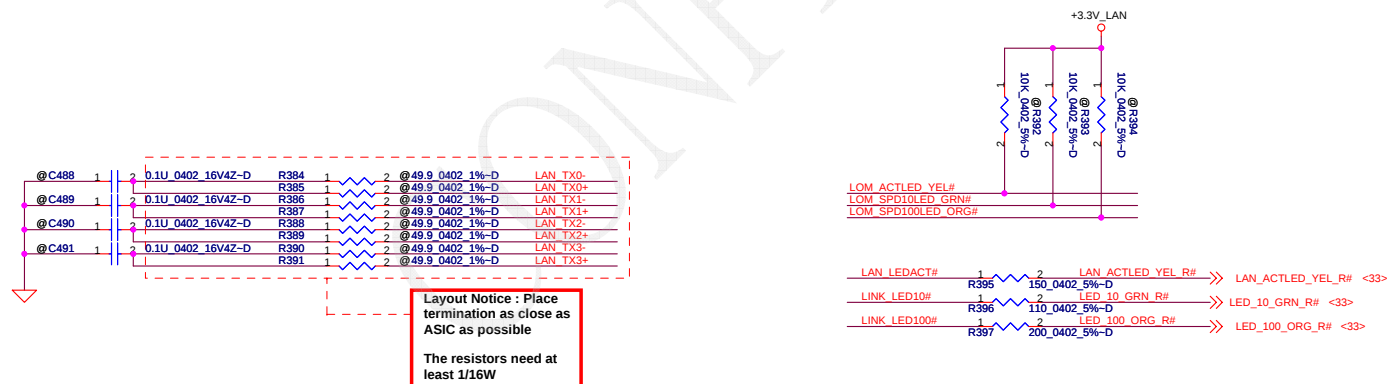
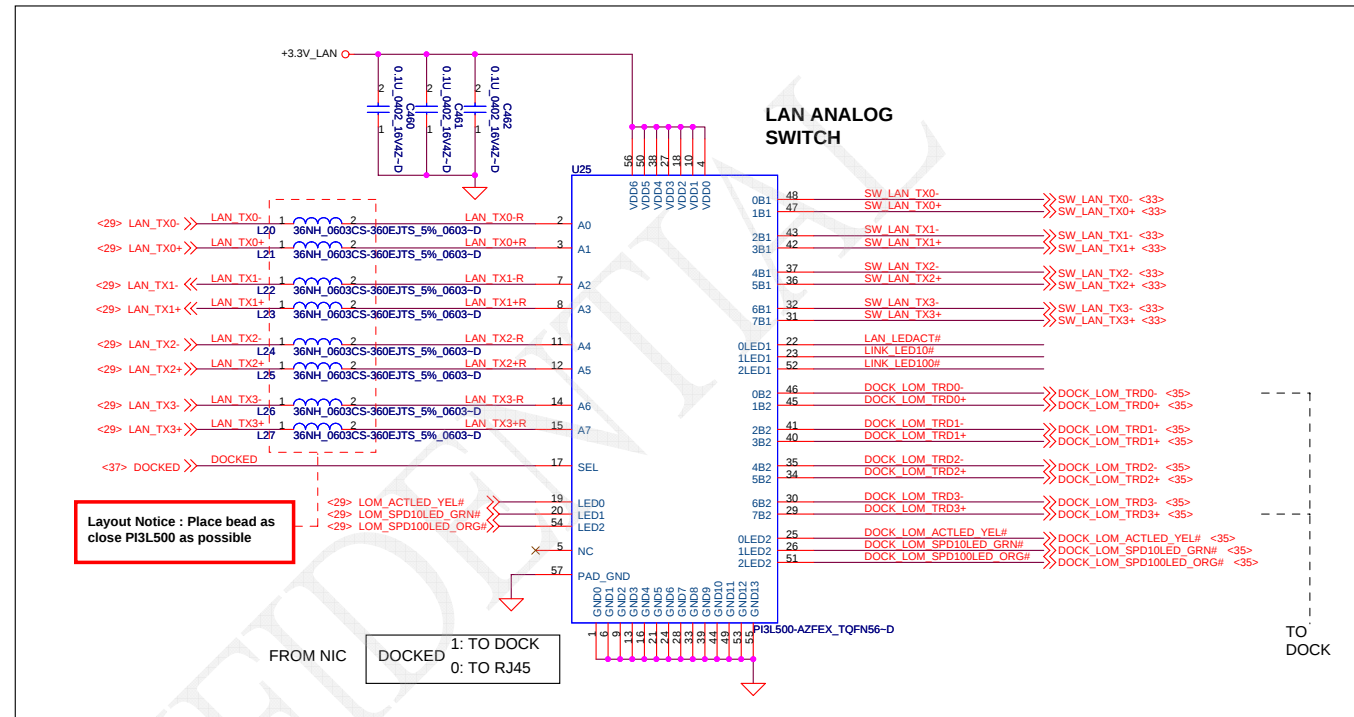
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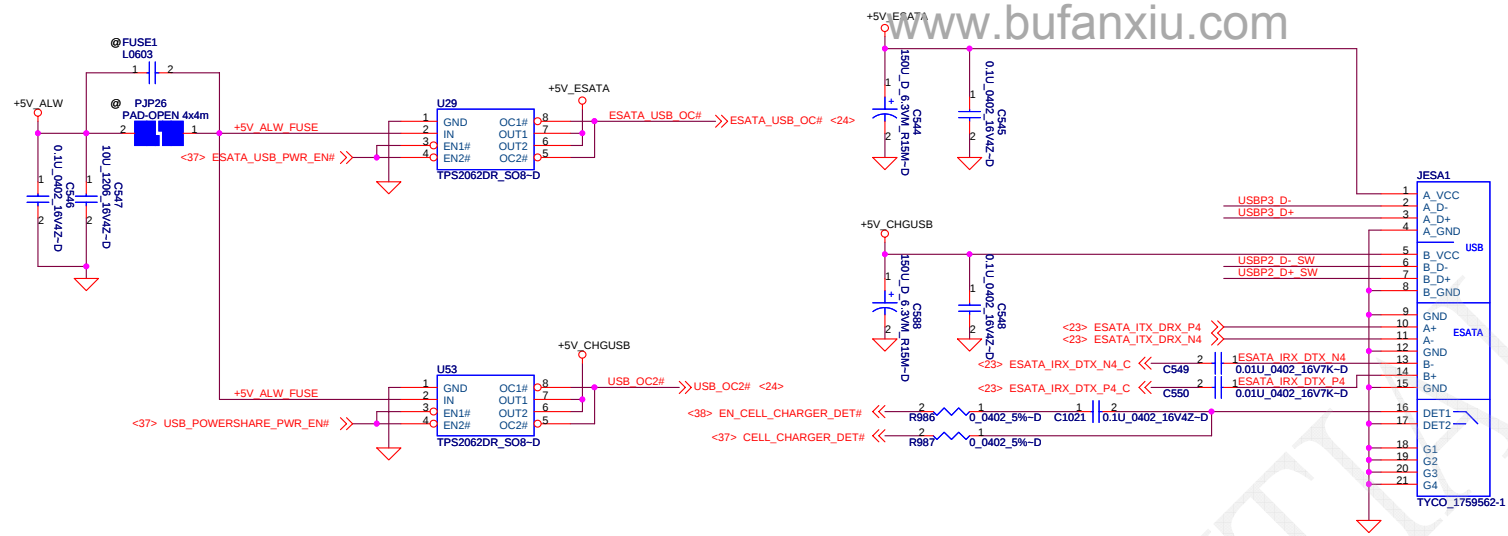
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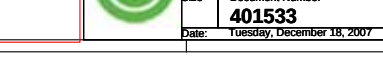
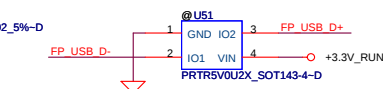
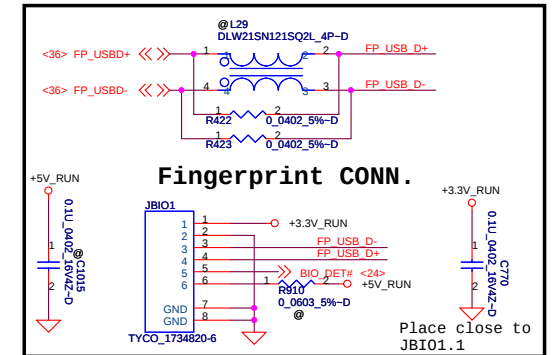
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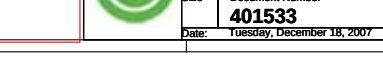
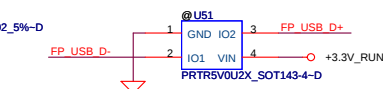
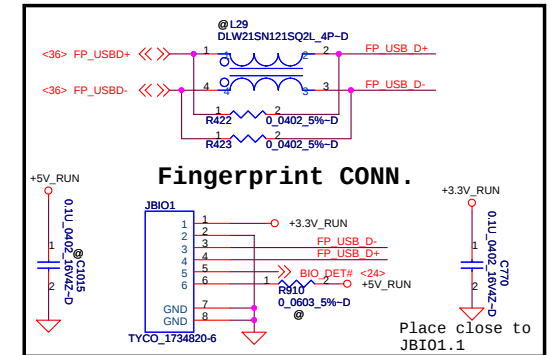




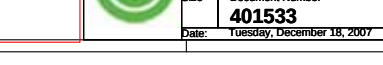
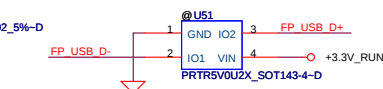
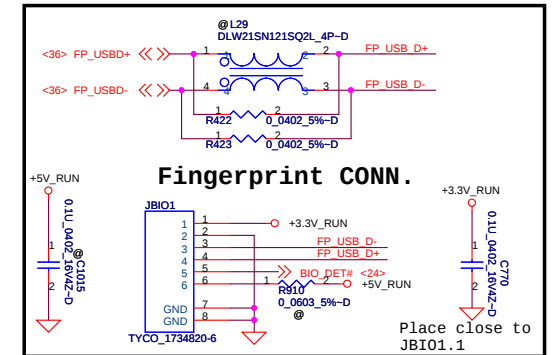
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0	JUSB1 (Ext Right Side Top)
1	JUSB1 (Ext Right Side Bottom)
2	JESA1 (Ext Left Side Bottom)
3	JESA1 (Ext Left Side TOP)
4	WLAN
5	WWAN
6	WPAN
7	Express card
8	DOCKING
9	DOCKING
10	USH->BIO
11	Camera



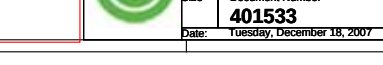
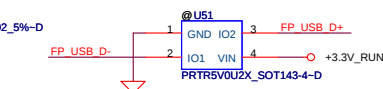
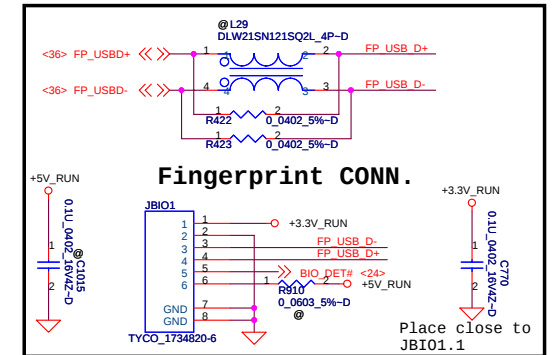
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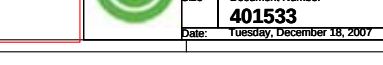
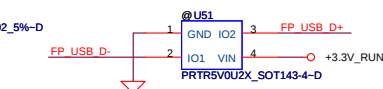
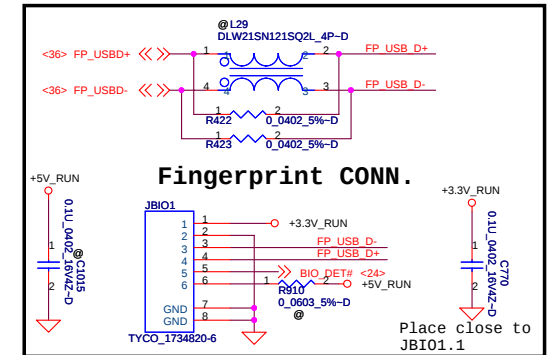
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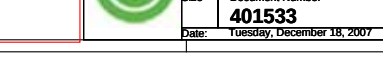
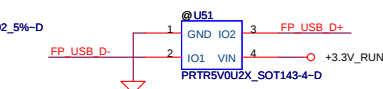
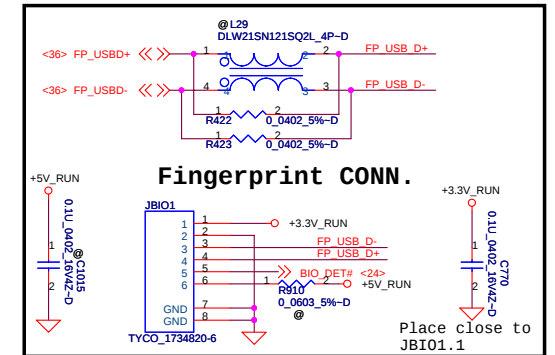
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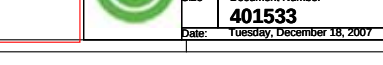
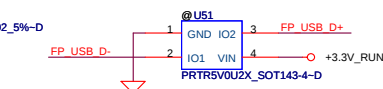
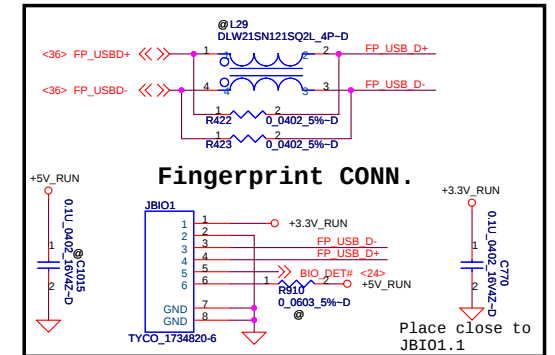
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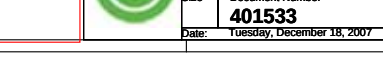
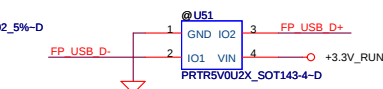
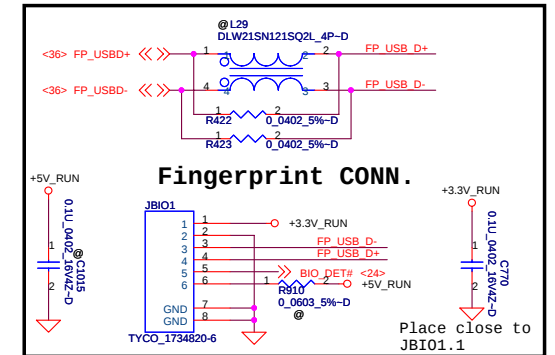
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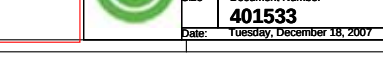
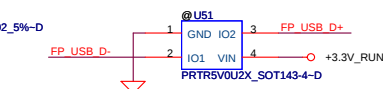
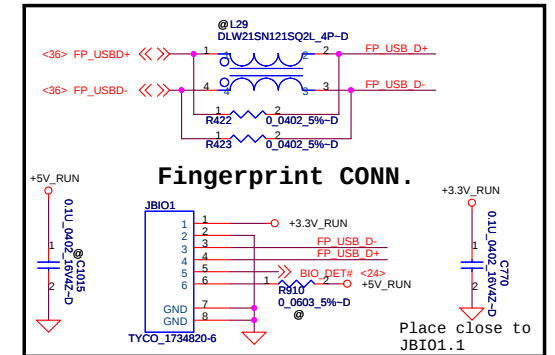
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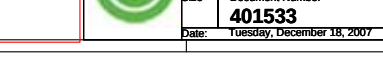
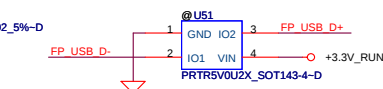
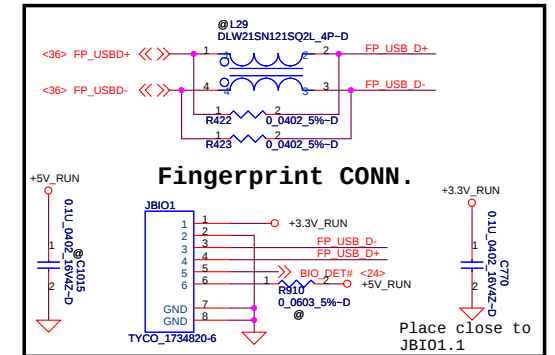
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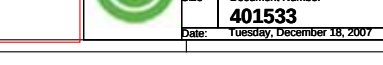
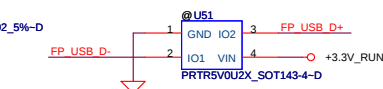
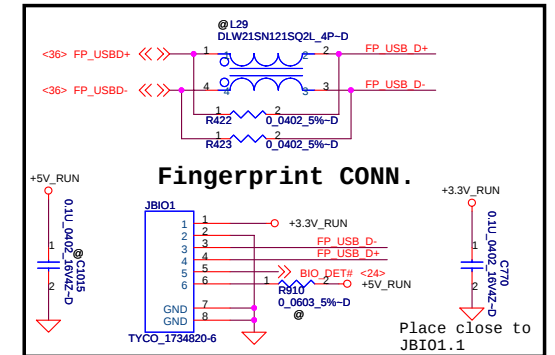
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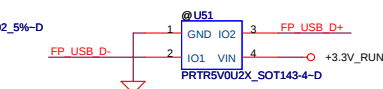
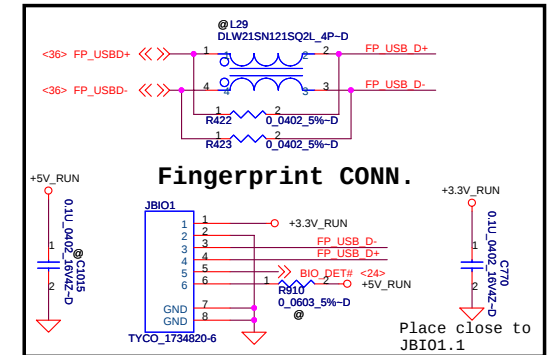
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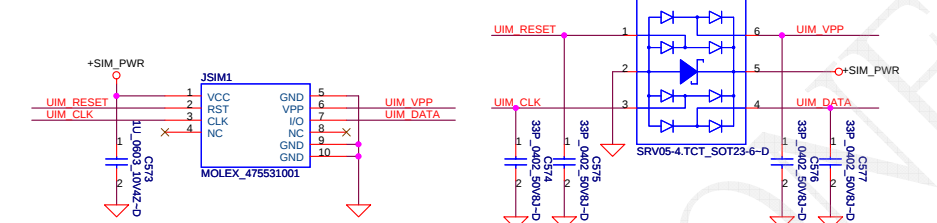
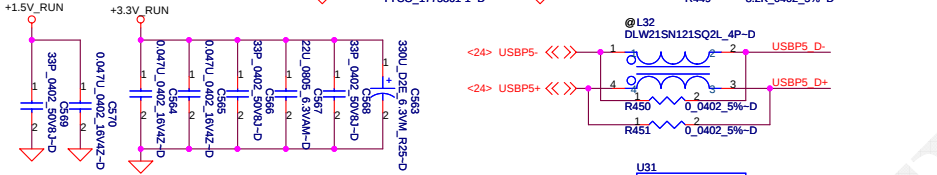
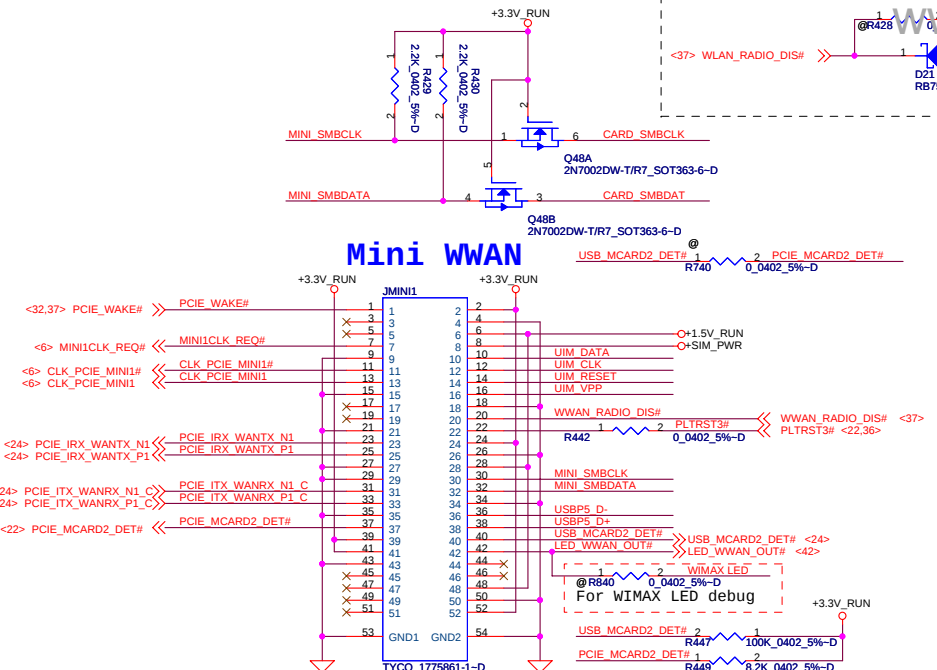


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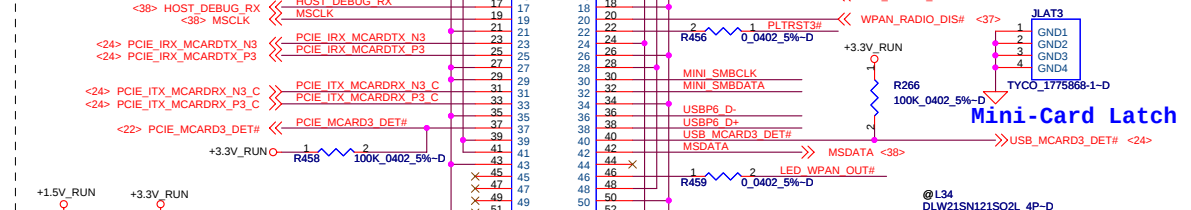
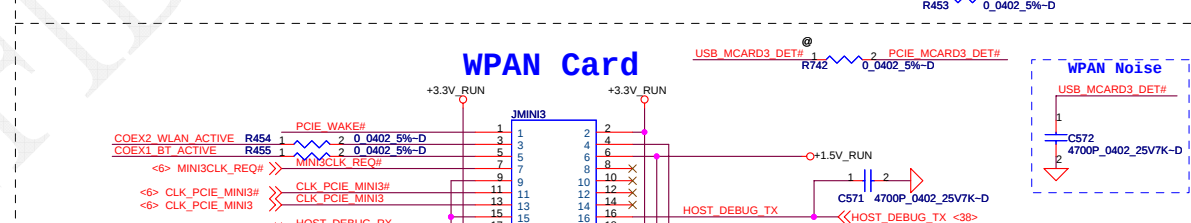
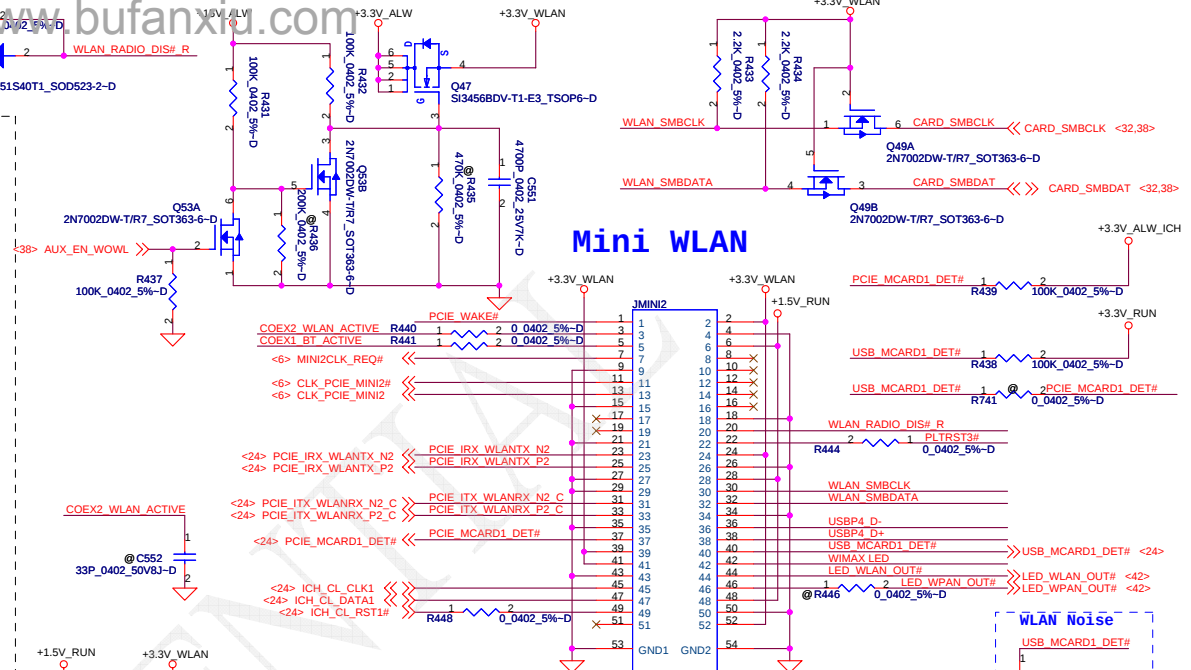


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PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+ -5%	500	375	NA



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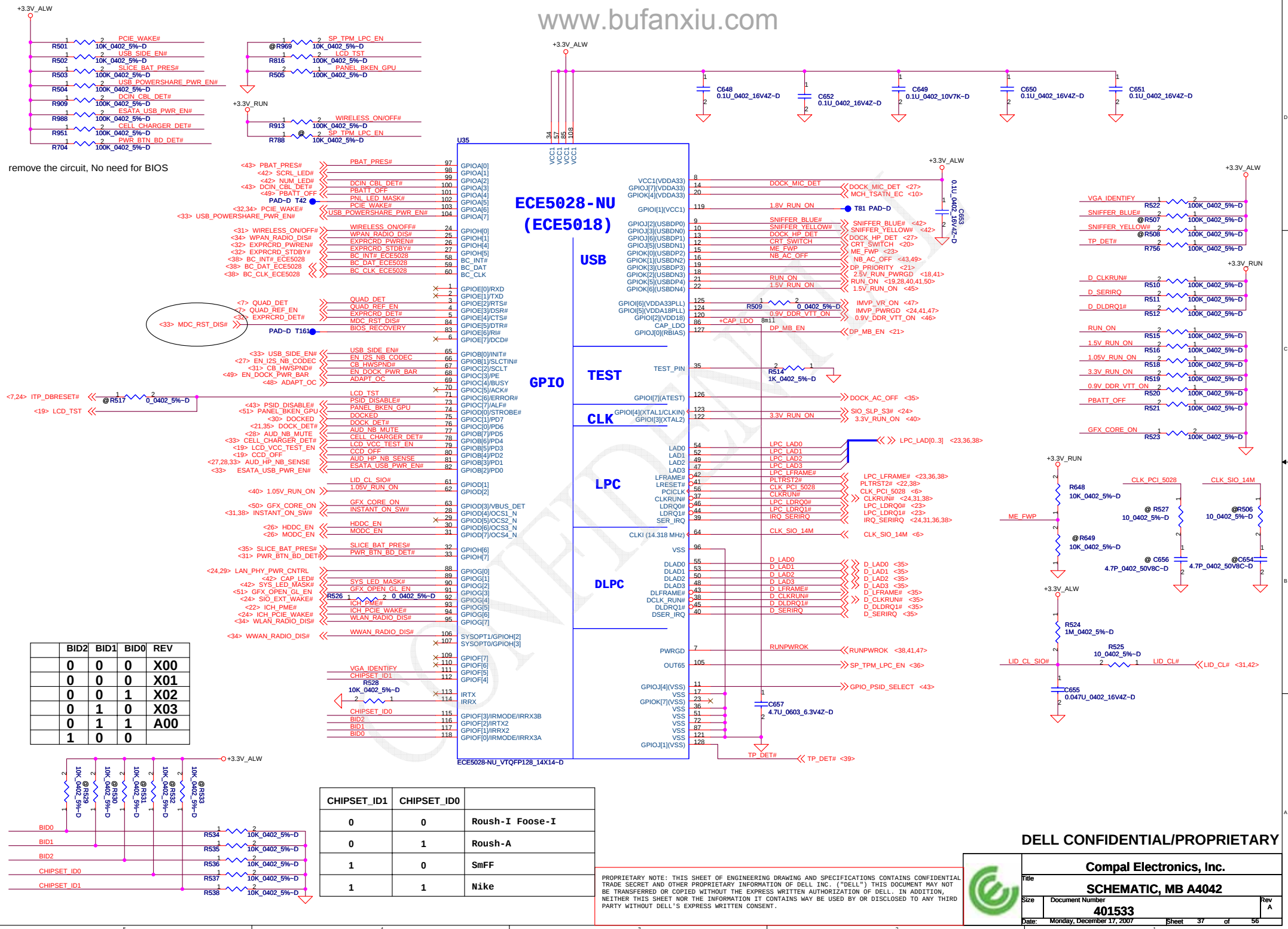
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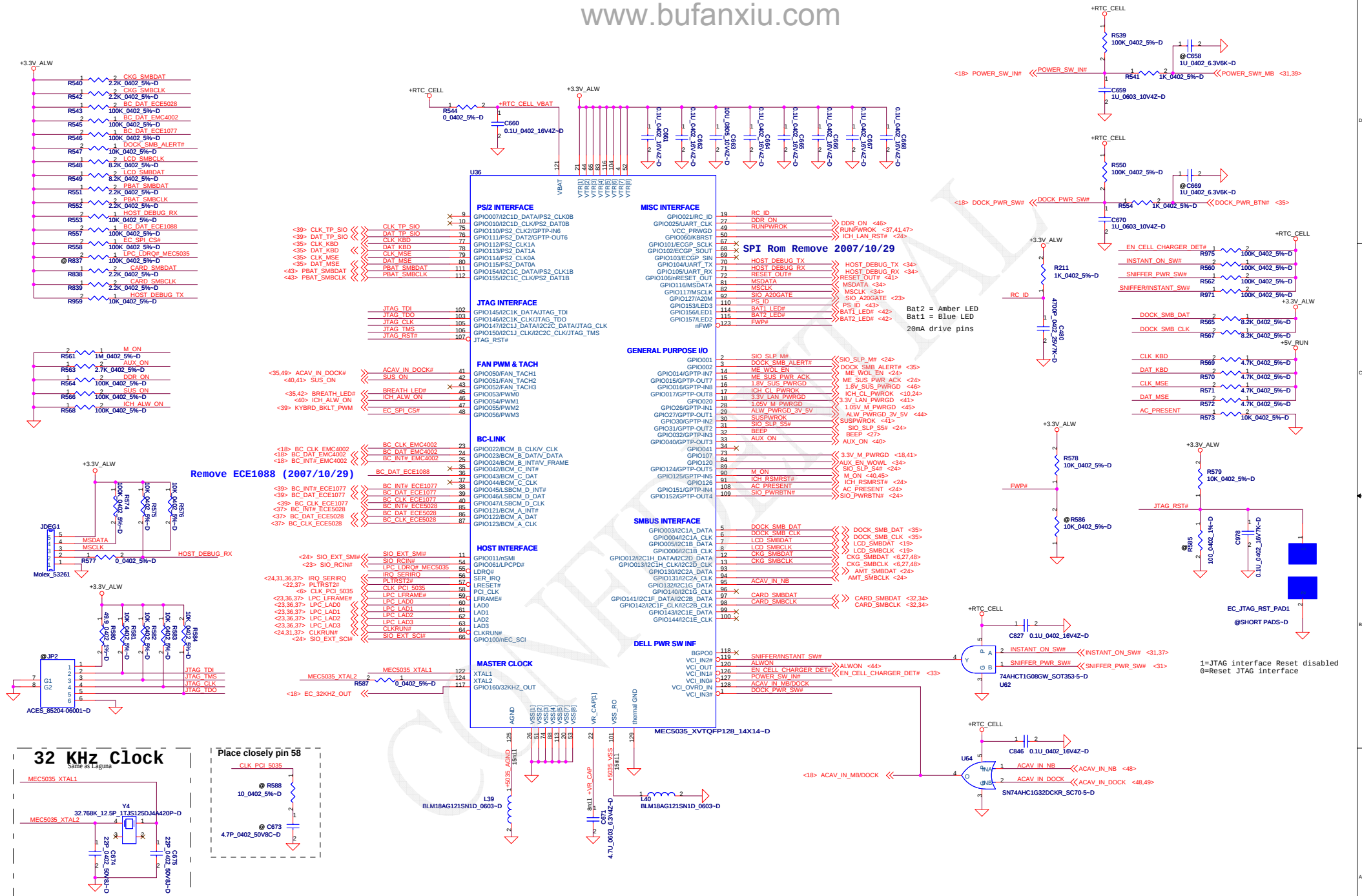
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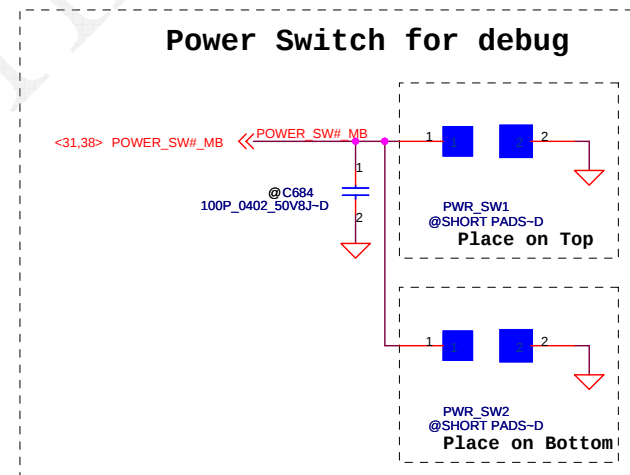
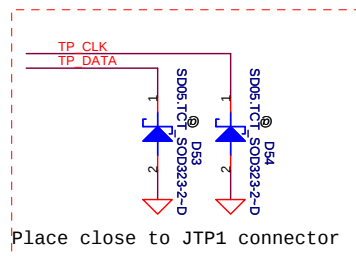
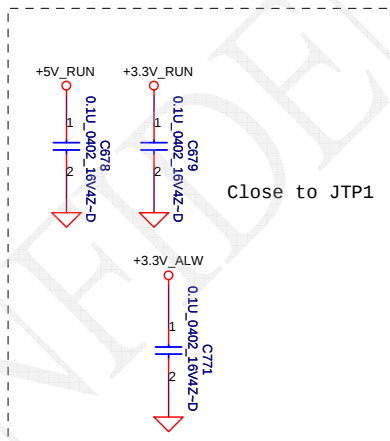
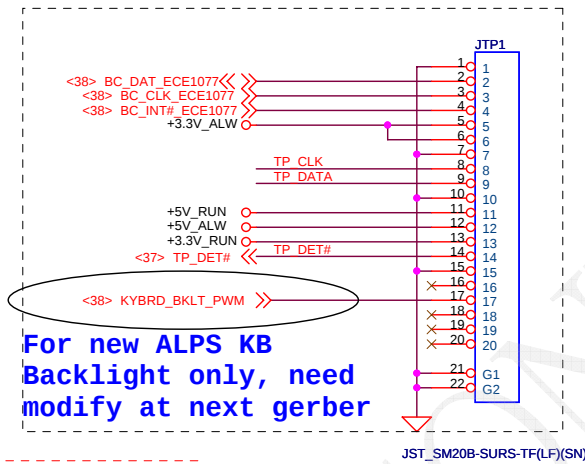
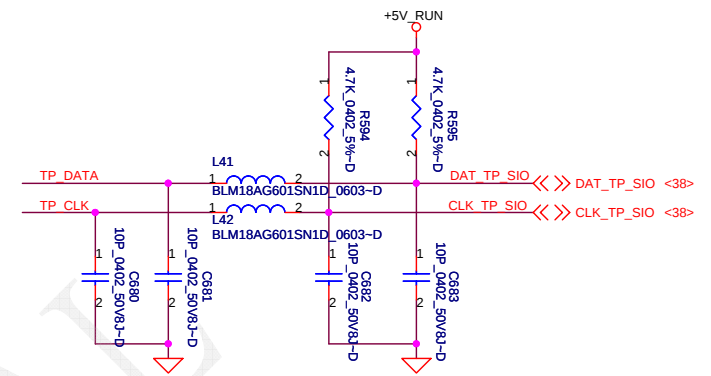
Monday, December 17, 2007

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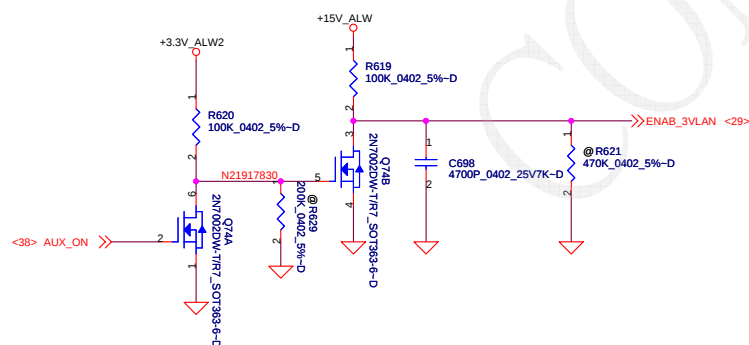
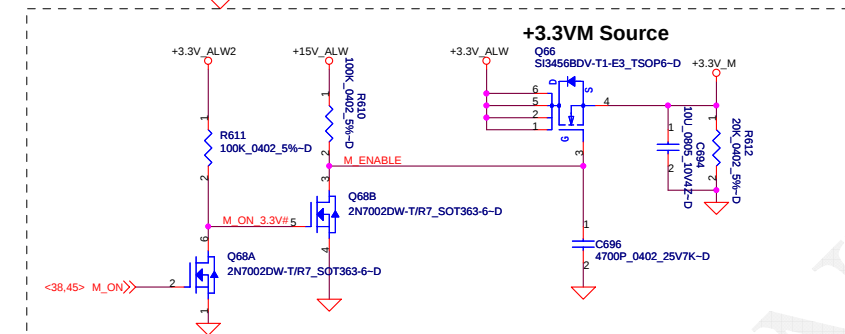
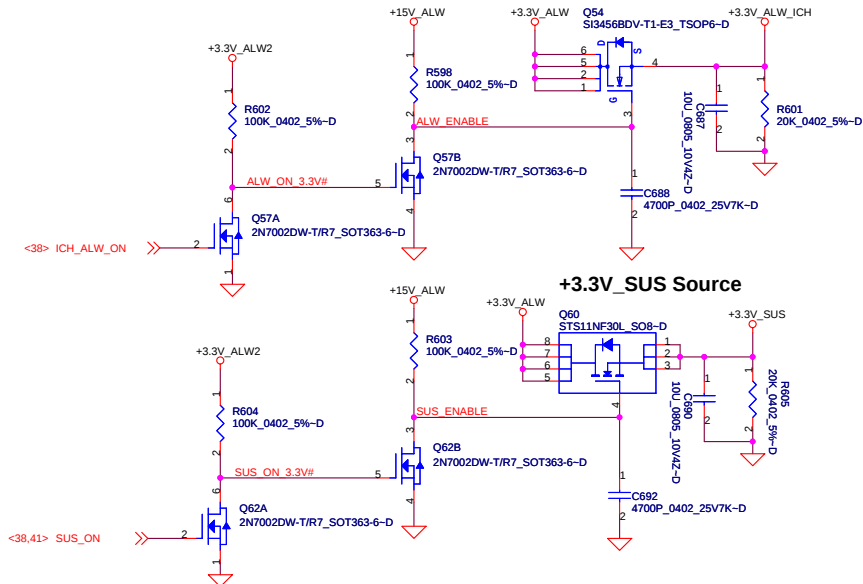
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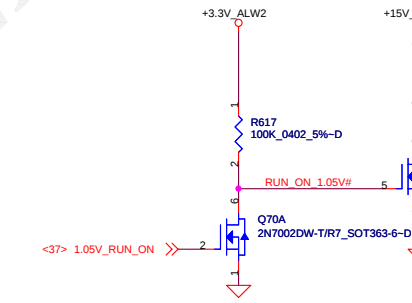
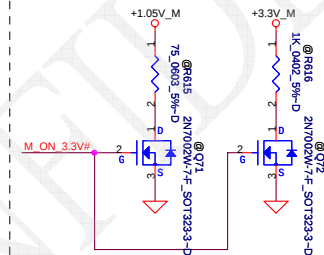
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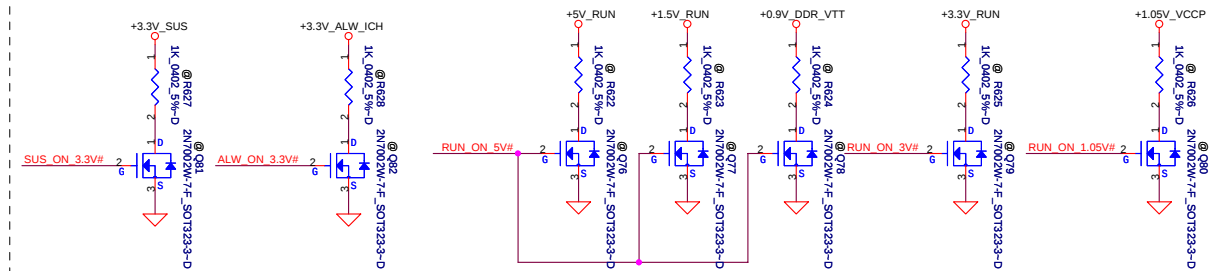
DC/DC Interface



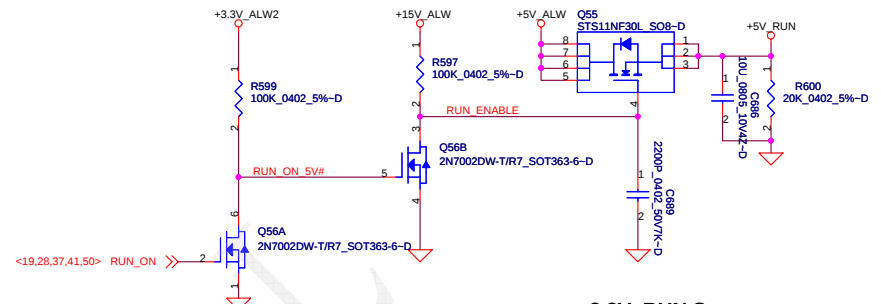
Discharge Circuit



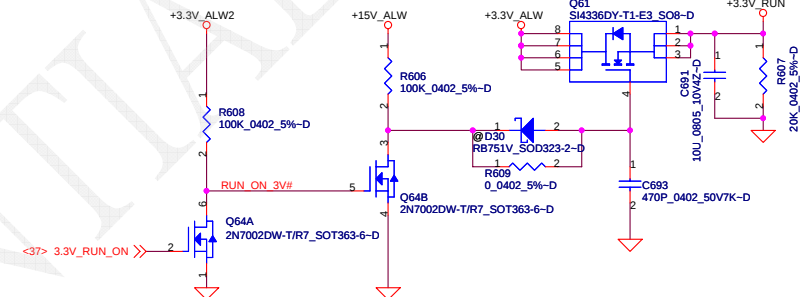
Discharge Circuit



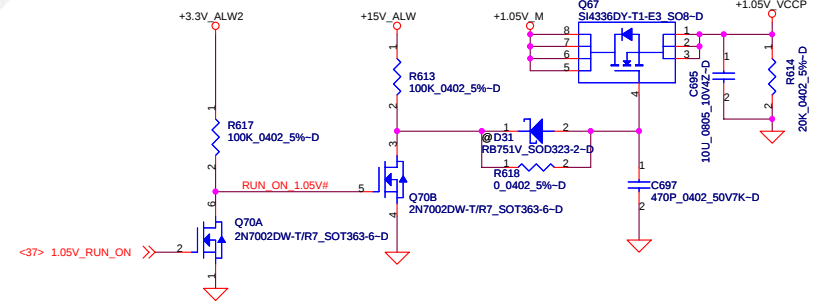
+5VRUN Source



+3.3V_RUN Source



+1.05V_VCCP Source



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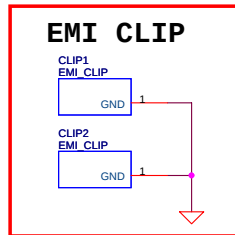
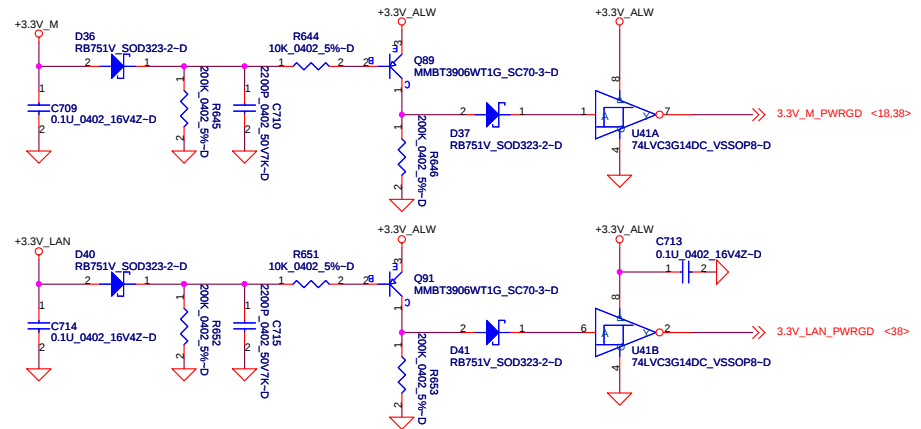
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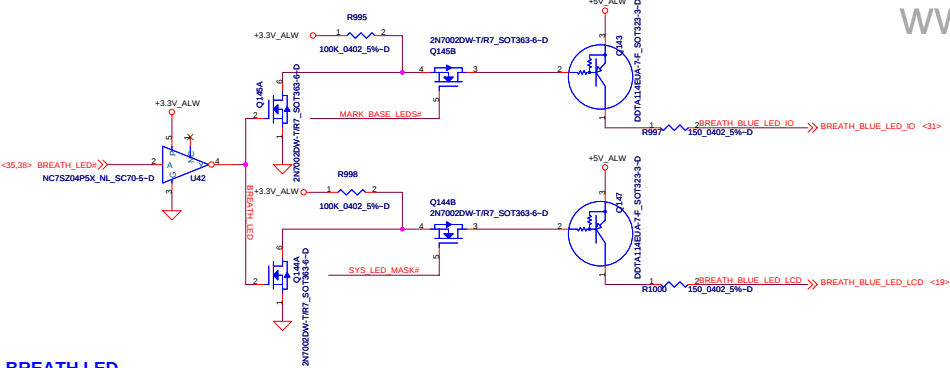
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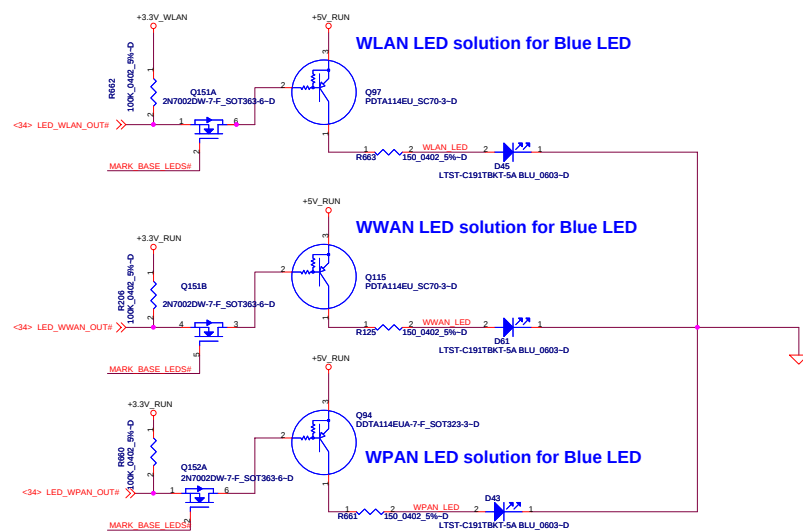
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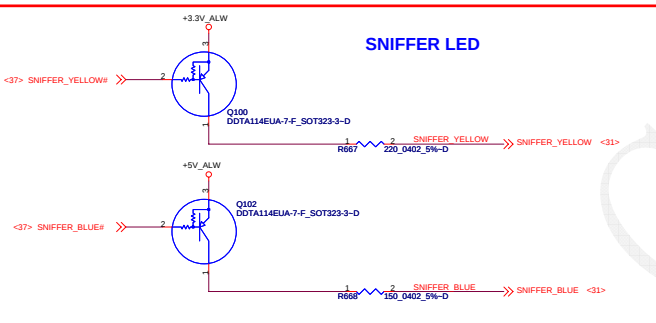
BREATH LED



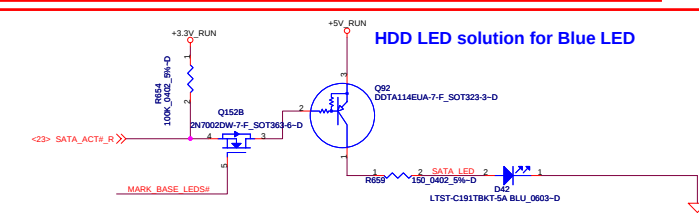
WLAN LED solution for Blue LED

WWAN LED solution for Blue LED

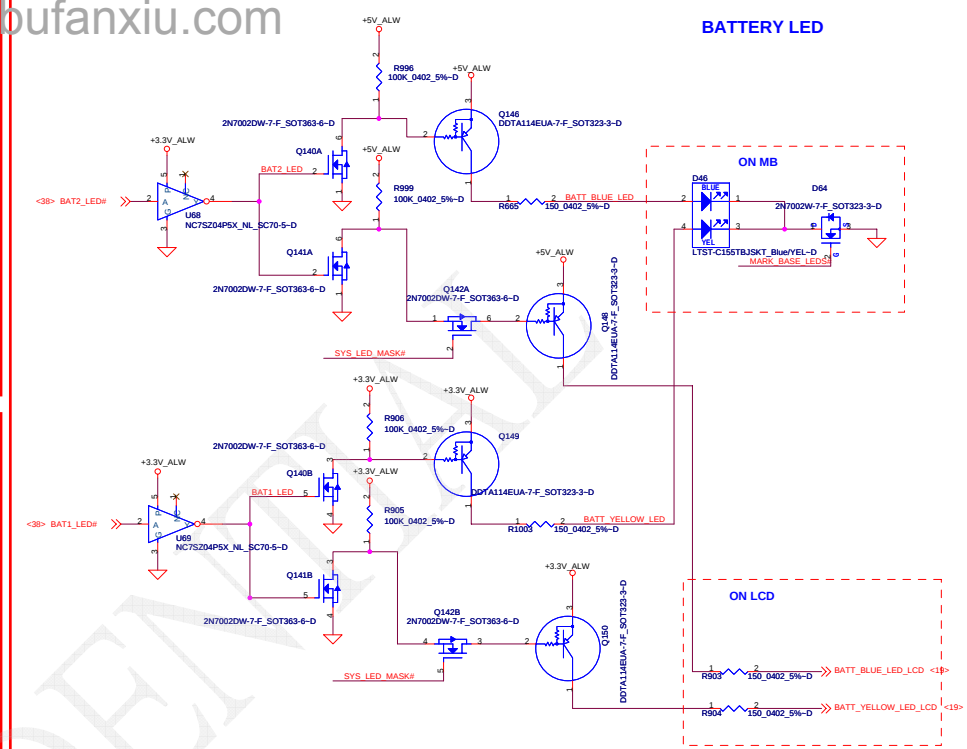
WPAN LED solution for Blue LED



SNIFFER LED



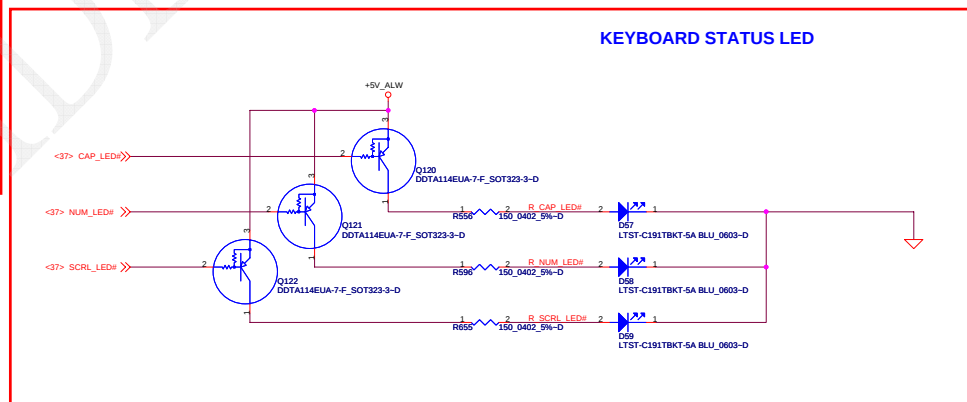
HDD LED solution for Blue LED



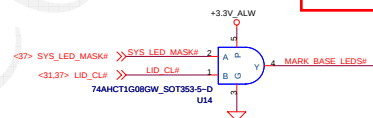
BATTERY LED

ON MB

ON LCD



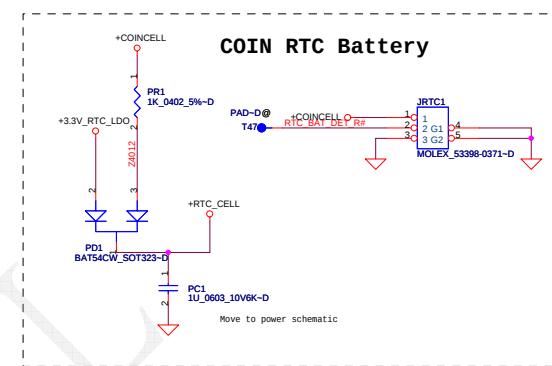
KEYBOARD STATUS LED



BIOS GPIO Table for LED Control

	SYS_LED_MASK#	LID_CL#
MARK ALL LED (SNIFFER FUNCTION)	Low	X
MARK BASE MB LEDs (Lid Closed)	High	Low
Do Not Mark LEDs (Lid Opened)	High	High

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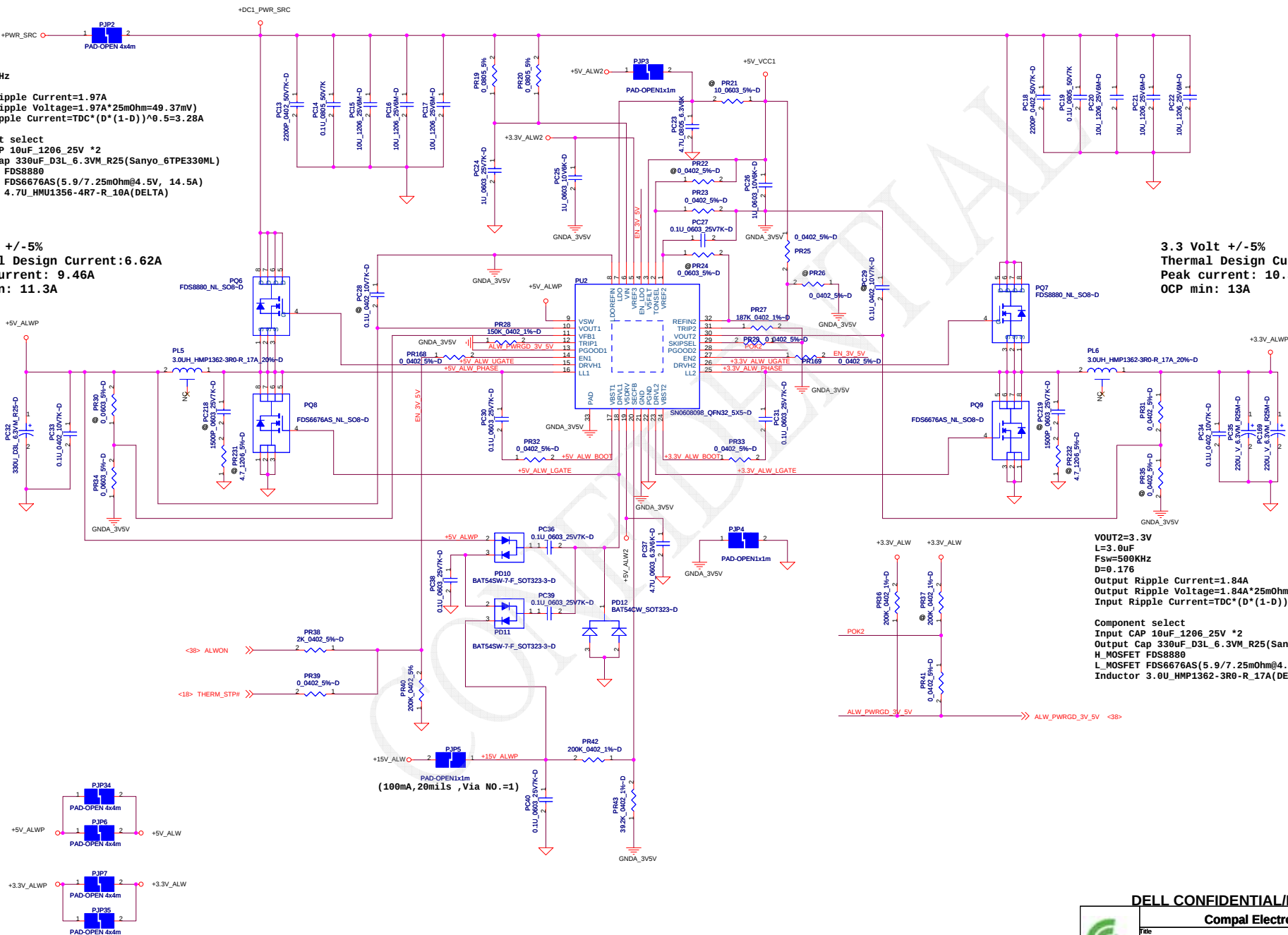
+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP

VOUT1=5V
L=4.7uF
Fsw=400KHz
D=0.265
Output Ripple Current=1.97A
Output Ripple Voltage=1.97A*25mOhm=49.37mV
Input Ripple Current=TDC*(D*(1-D))^0.5=3.28A

Component select
Input CAP 10uF 1206 25V *2
Output Cap 330uF_D3L 6.3VM_R25(Sanyo_6TPE330ML)
H_MOSFET FDS8880
L_MOSFET FDS6676AS(5.9/7.25mOhm@4.5V, 14.5A)
Inductor 4.7U_HMU1356-4R7-R_10A(DELTA)

5 Volt +/-5%
Thermal Design Current:6.62A
Peck current: 9.46A
OCP min: 11.3A

3.3 Volt +/-5%
Thermal Design Current: 7.39A
Peak current: 10.56A
OCP min: 13A



VOUT2=3.3V
L=3.0uF
Fsw=500KHz
D=0.176
Output Ripple Current=1.84A
Output Ripple Voltage=1.84A*25mOhm=46.05mV
Input Ripple Current=TDC*(D*(1-D))^0.5=3.28A

Component select
Input CAP 10uF 1206 25V *2
Output Cap 330uF_D3L 6.3VM_R25(Sanyo_6TPE330ML)
H_MOSFET FDS8880
L_MOSFET FDS6676AS(5.9/7.25mOhm@4.5V, 14.5A)
Inductor 3.0U_HMP1362-3R0-R_17A(DELTA)

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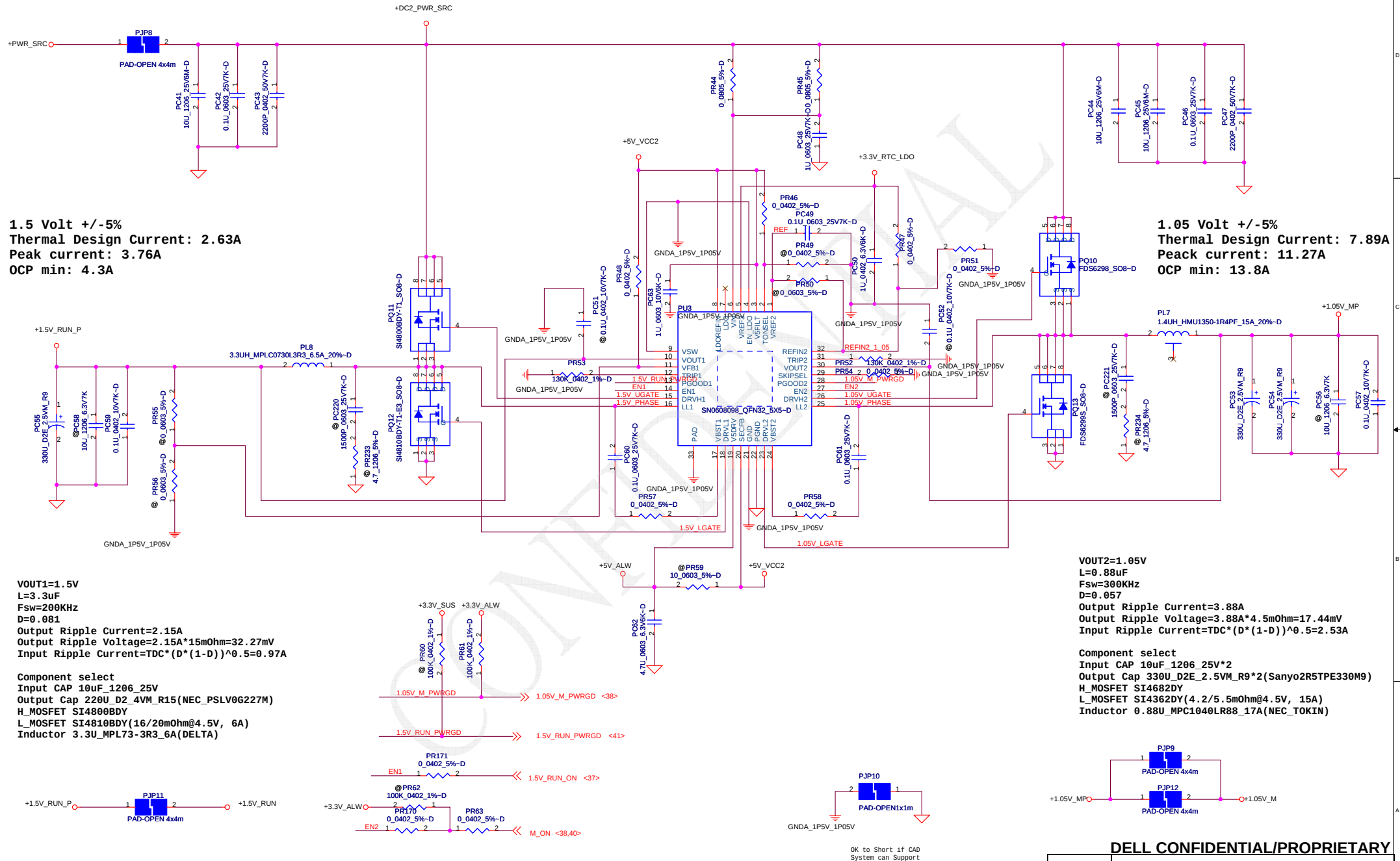
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+1.5V_RUN / +1.05V_M / +3.3V_RTC_LDO



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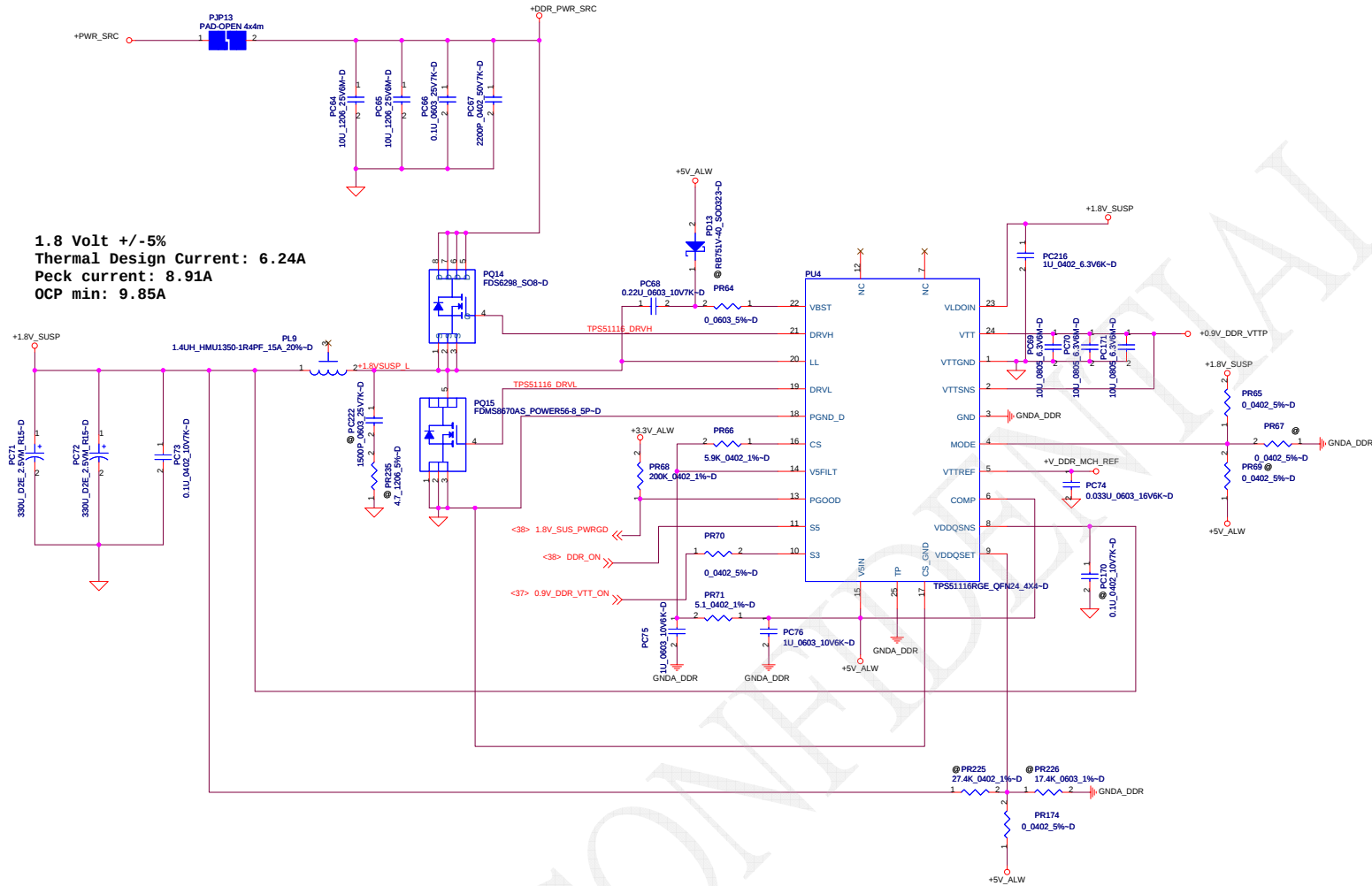
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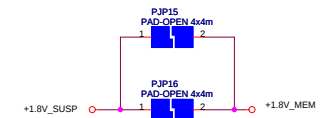
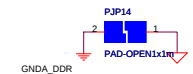
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+1.8VSUSP/ +0.9V_DDR_VTT DDR2 Termination

1.8 Volt +/-5%
Thermal Design Current: 6.24A
Peck current: 8.91A
OCP min: 9.85A



Design current 0.7A for +0.9V_DDR_VTTP
Peak current 1A for +0.9V_DDR_VTTP



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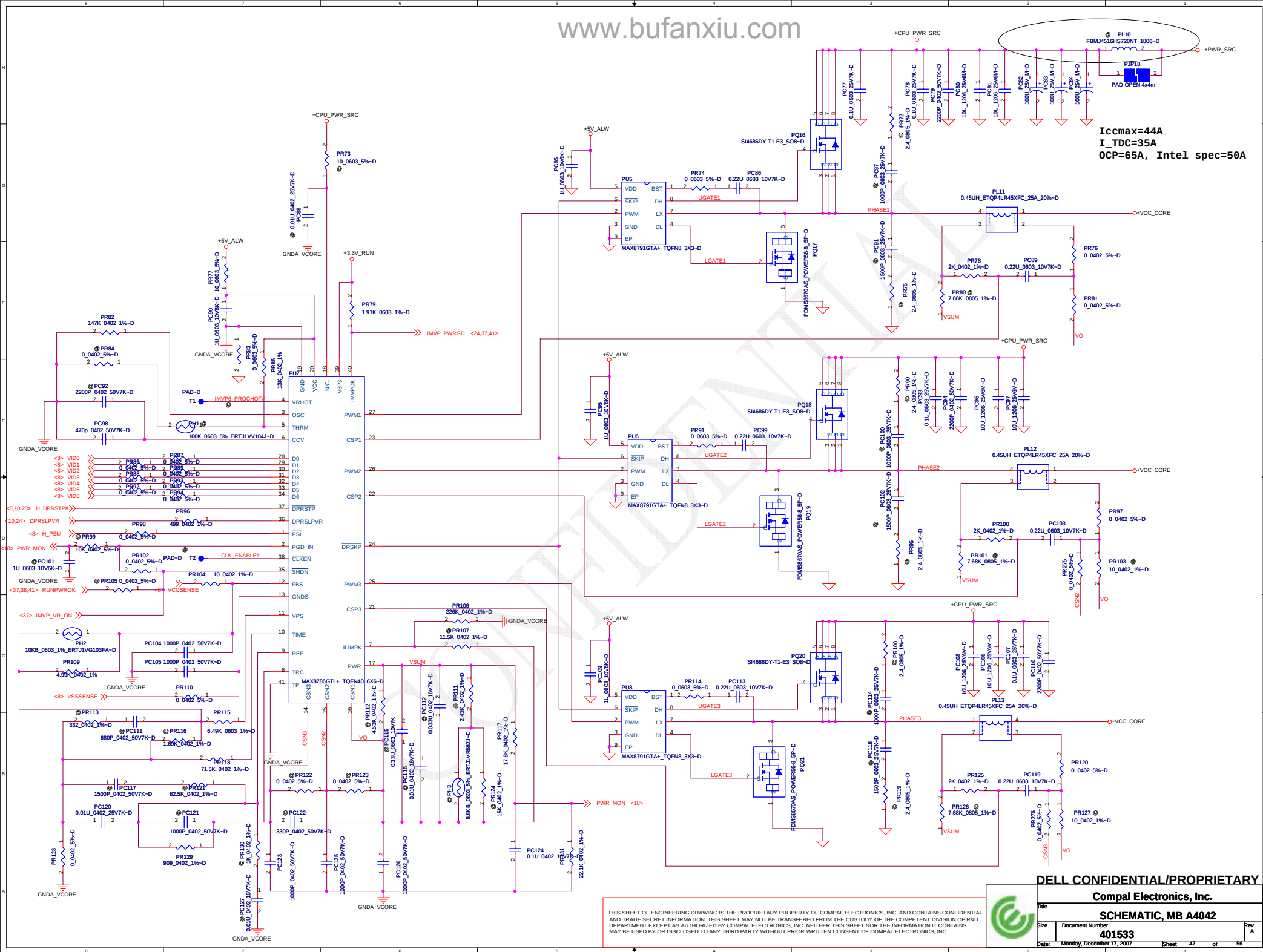
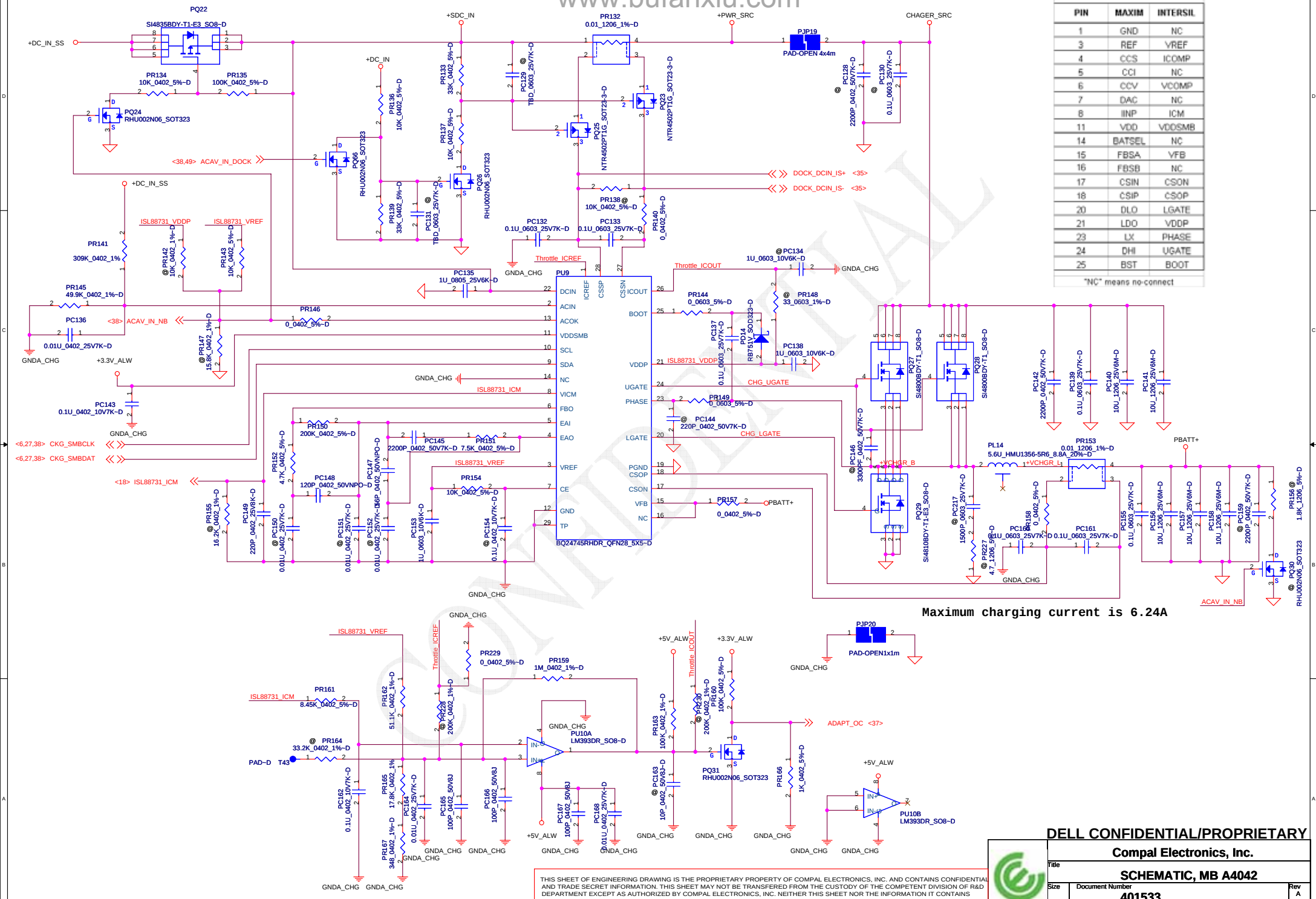


TABLE 3, PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
"NC" means no-connect		



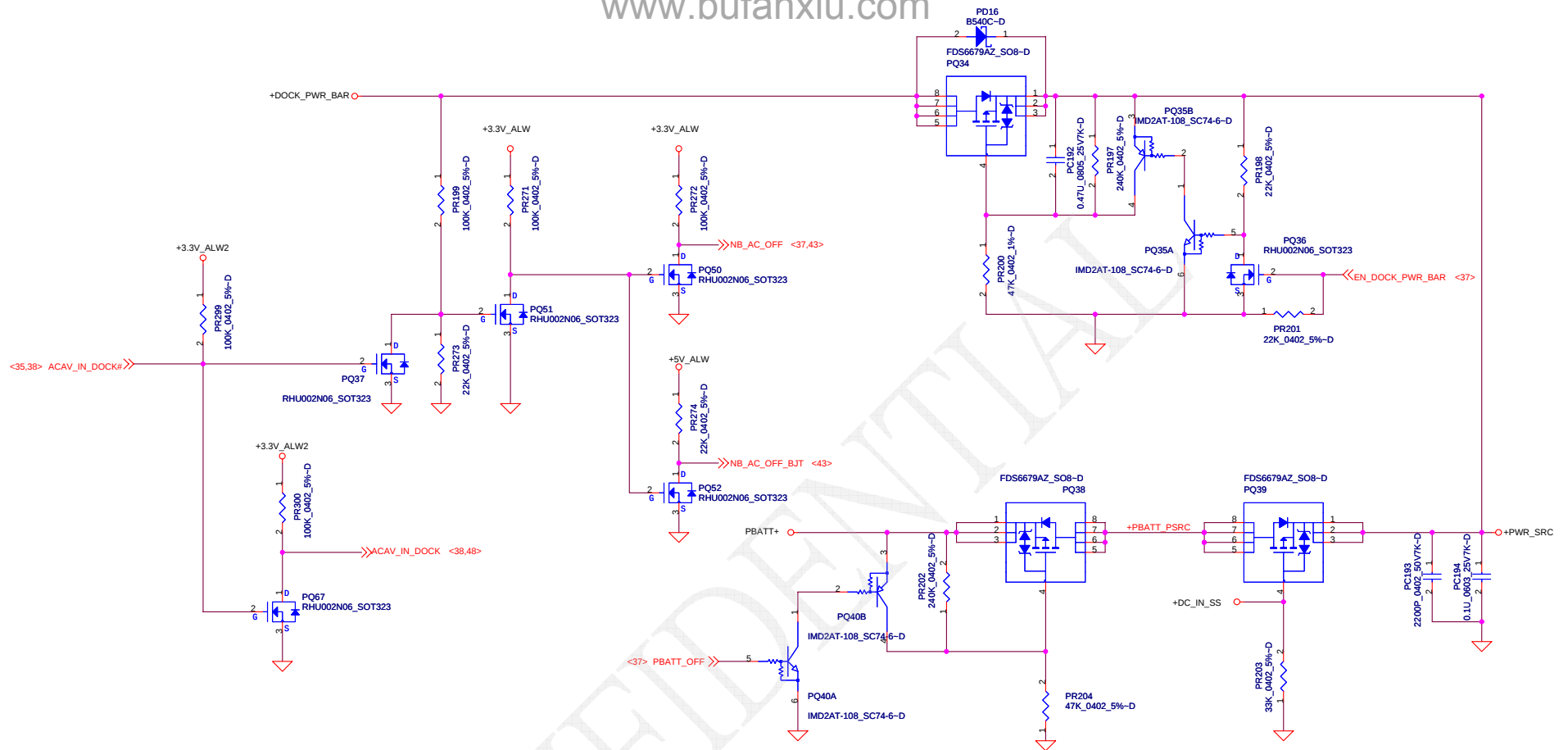
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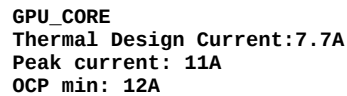
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output voltage adjustable network

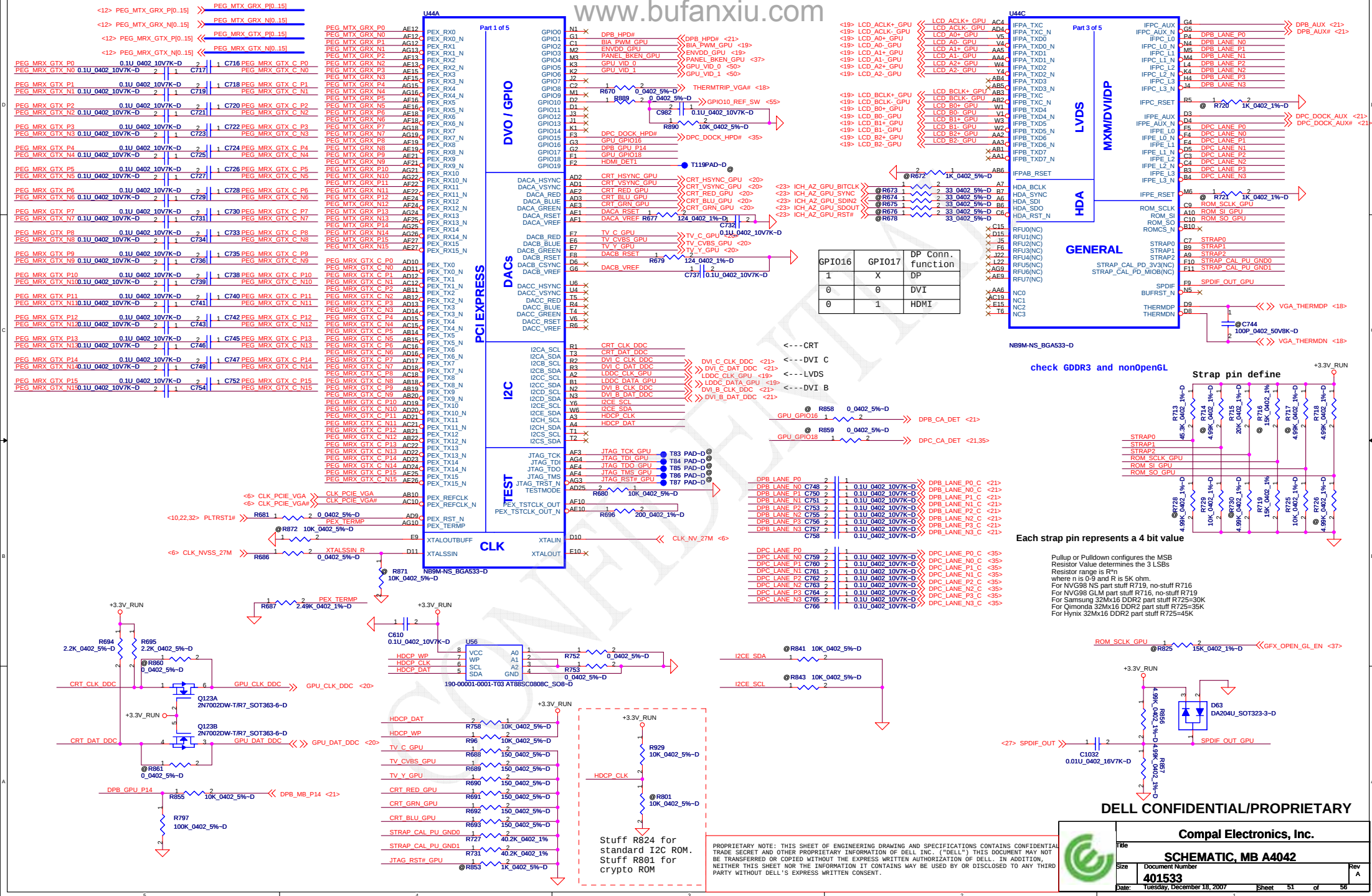
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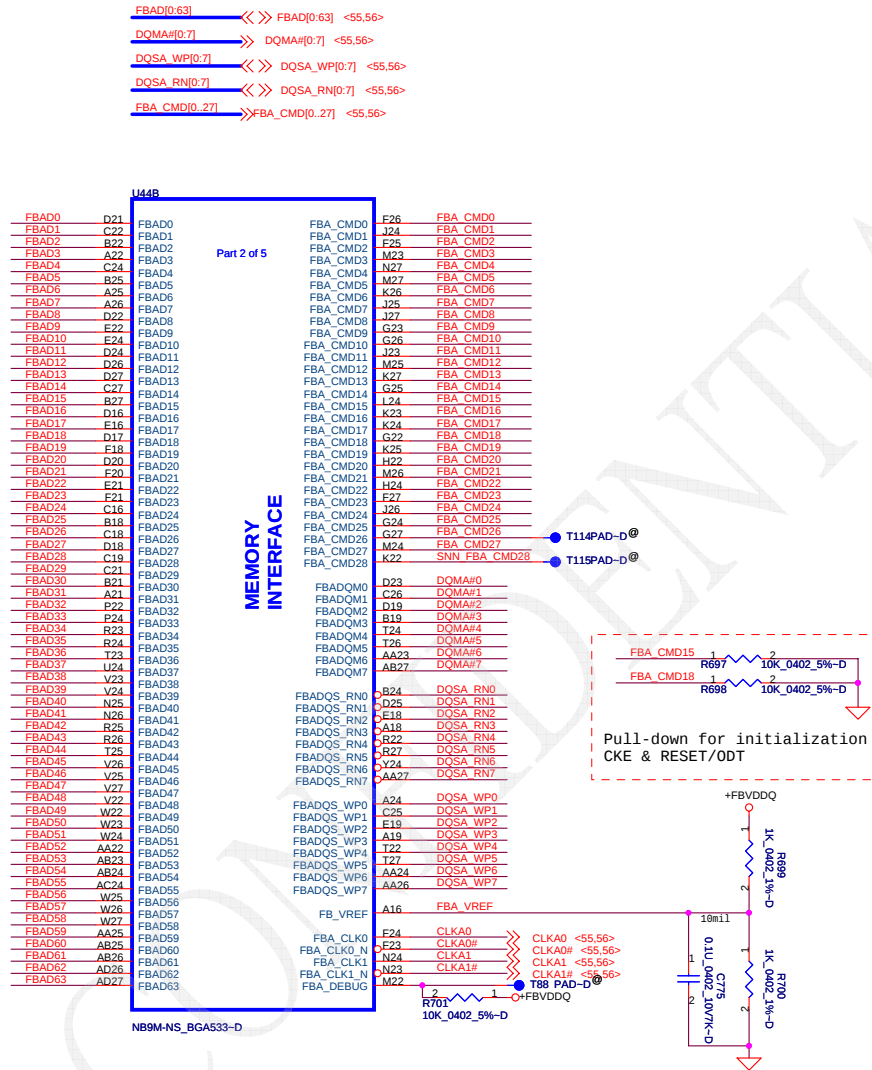
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	0..31	32..63
FBA_CMD0	A4	
FBA_CMD1	RAS#	RAS#
FBA_CMD2	A5	
FBA_CMD3	BA1	BA1
FBA_CMD4		A2
FBA_CMD5		A4
FBA_CMD6		A3
FBA_CMD7	CS1#	CS1#
FBA_CMD8	CS0#	CS0#
FBA_CMD9	A11	A11
FBA_CMD10	CAS#	CAS#
FBA_CMD11	WE#	WE#
FBA_CMD12	BA0	BA0
FBA_CMD13		A5
FBA_CMD14	A12	A12
FBA_CMD15	RST/ODT	RST/ODT
FBA_CMD16	A7	A7
FBA_CMD17	A10	A10
FBA_CMD18	CKE	CKE
FBA_CMD19	A0	A0
FBA_CMD20	A9	A9
FBA_CMD21	A6	A6
FBA_CMD22	A2	
FBA_CMD23	A8	A8
FBA_CMD24	A3	
FBA_CMD25	A1	A1
FBA_CMD26	A13	A13
FBA_CMD27	BA2	BA2
FBA_CMD28	RFU0	RFU0
FBA_CMD29	RFU1	RFU1
FBA_CMD30	RFU2	RFU2

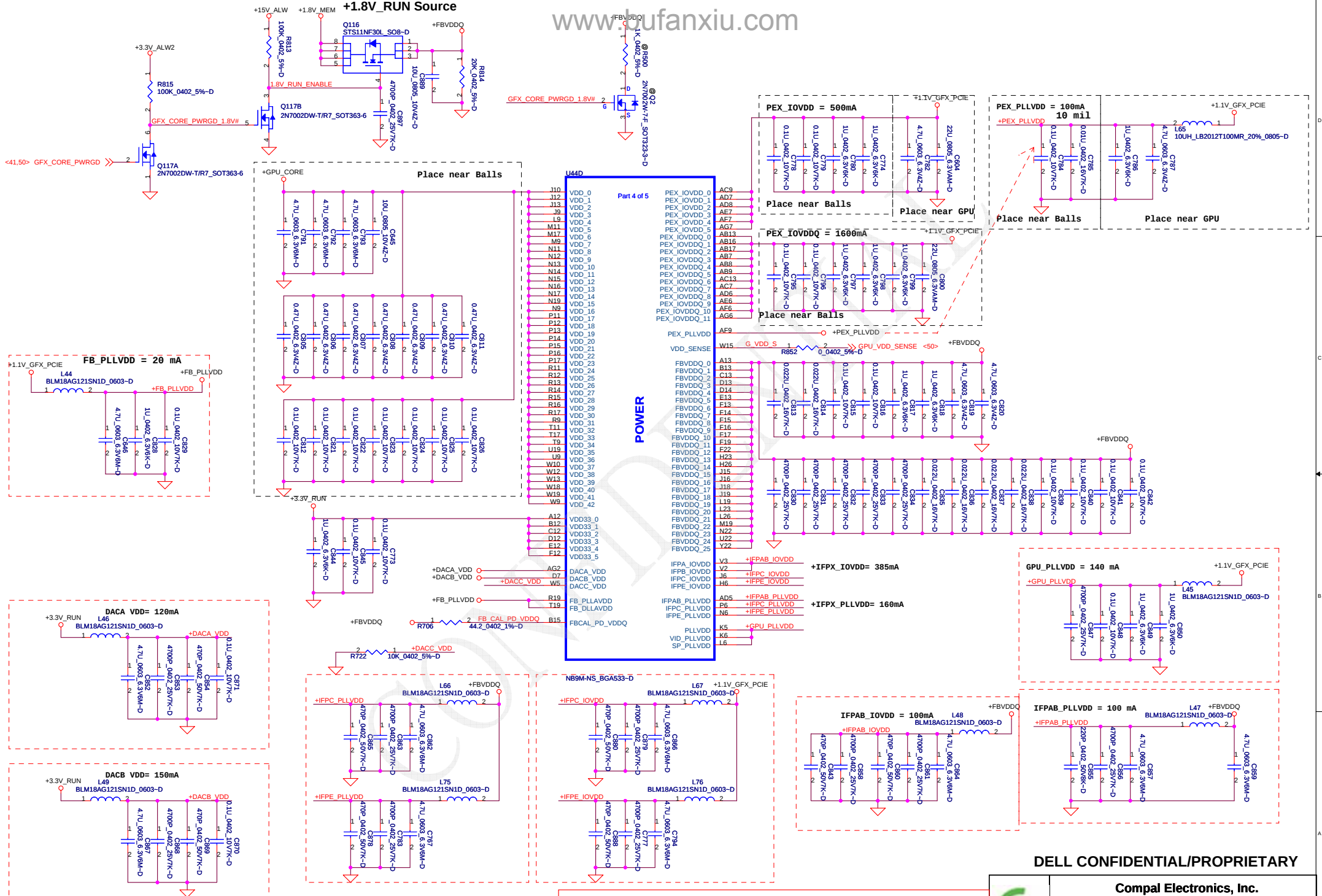
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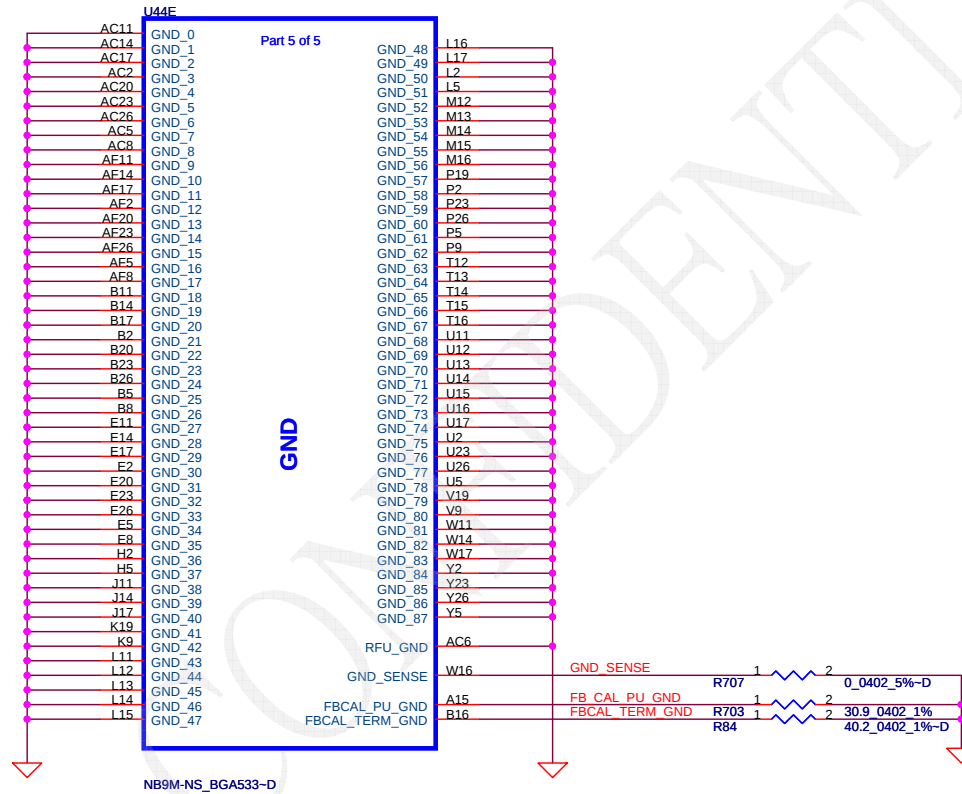


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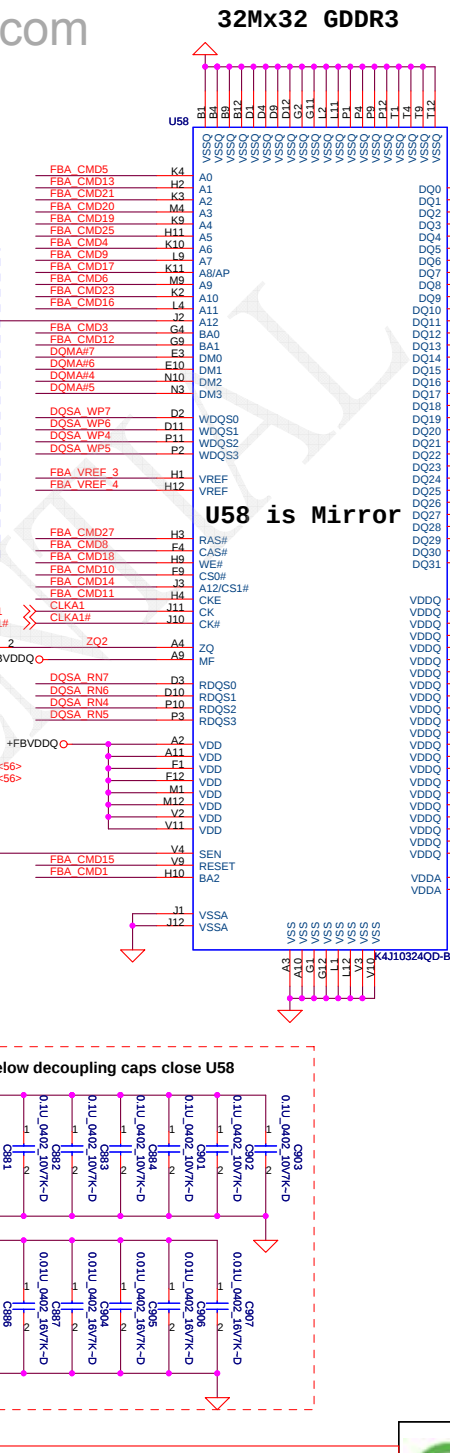
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```

RAS#  --> BA2
CAS#  --> CS0#
WE    --> CKE
CS0#  --> CAS#
A0    --> A0
A1    --> A5
A2    --> A6
A3    --> A9
A4    --> A0
A5    --> A1
A6    --> A2
A7    --> A11
A8    --> A10
A9    --> A3
A10   --> A8
A11   --> A7
CKE   --> WE#
BA0   --> BA1
BA1   --> BA0
BA2   --> RAS#
NC/CS1#  --> NV/CS1#

```

T4C

T

U60
K4J103240D-BC12 FBGA136-D

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<u>DQSA_RN[0..7]</u>	<< >>	DQSA_RN[0..7]	<52,55>
<u>DQMA# [0..7]</u>	<<	DQMA# [0..7]	<52,55>
<u>FBA_CMD[0..27]</u>	>>	FBA_CMD[0..27]	<52,55>

FBAD9
FBAD8
FBAD14
FBAD15
FBAD12
FBAD11
FBAD10
FBAD13

FBA VREF 3
FBA VREF 4

FBA_CMD1	H3	RAS#
FBA_CMD10	F4	CAS#
FBA_CMD11	H9	WE#
FBA_CMD7	F9	CS0#
FBA_CMD14	12	

FBA_CMD18	H4	A12/CS1#
CLKA1	J11	CKE
CLKA1#	J10	CK
		CK#
ZQ4	A4	ZQ
	A9	MF
DQSA RN6	D3	RDQS0
DQSA RN7	D10	RDQS1
DQSA RN5	P10	RDQS2
DQSA RN4	P3	RDQS3

AVDDQ

A2	VDD
A11	VDD
F1	VDD
F12	VDD
M1	VDD
M12	VDD
V2	VDD
V11	VDD
V4	SEN
FBA_CMD15	RESET
FBA_CMD27	BA2

FBA_VREF_3	>>	FBA_VREF_3 <5>
FBA_VREF_4	>>	FBA_VREF_4 <5>

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